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THE WORLDWIDE TECHNOLOGY WEEKLY

OCTOBER 14, 1985

THE SHIFT IN STRATEGY AT SILICON COMPILERS

WHY NOW?

PAGE 44

EWLETT-PACKARD TRIES TO GET ITS CAE ACT TOGETHER/40

ECHNOLOGY UPDATE 2: SEMICONDUCTORS IN FERMENT/55

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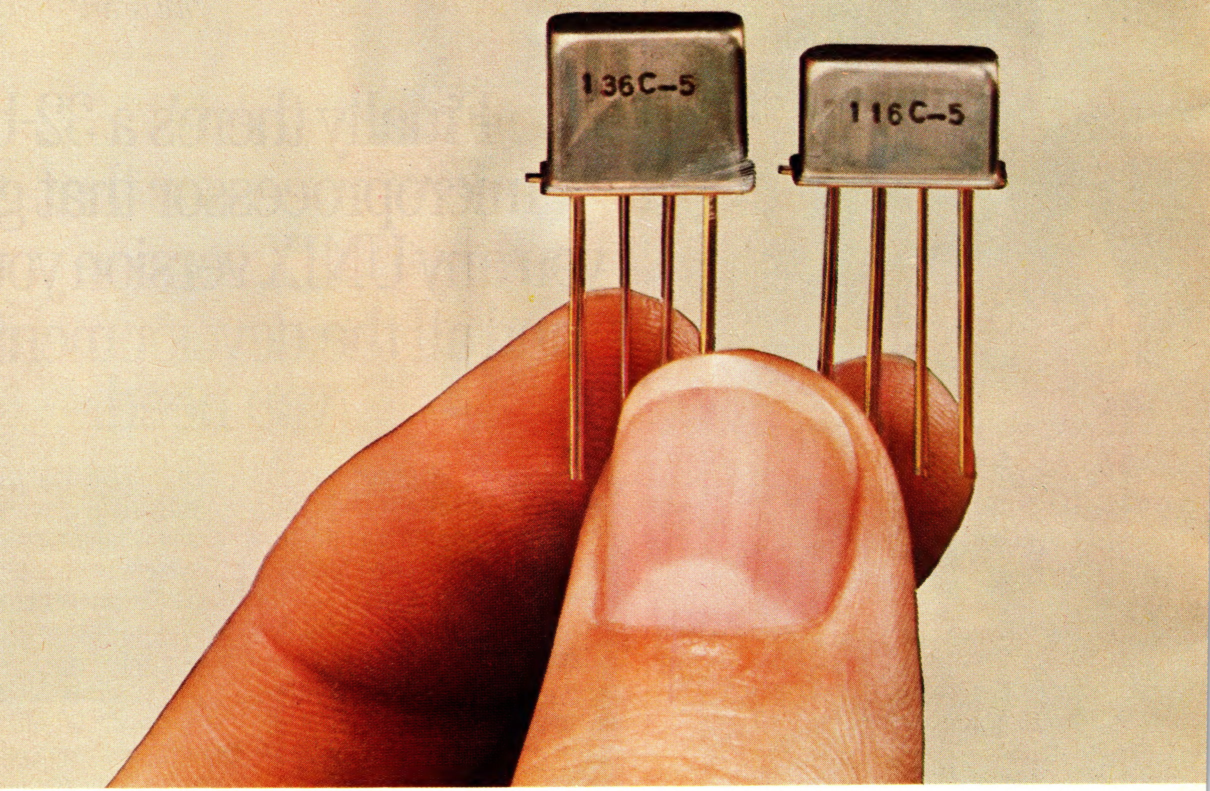

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Electronics

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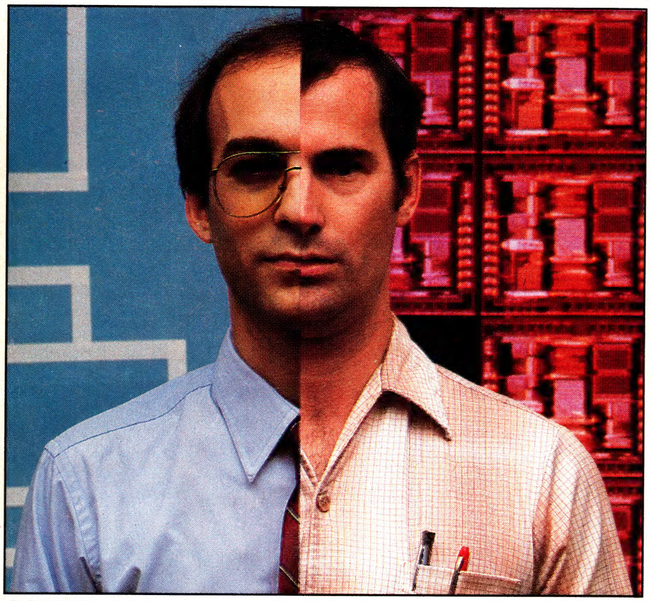

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Cover by Fred Sklenar, photograph by Walter Chrynwski

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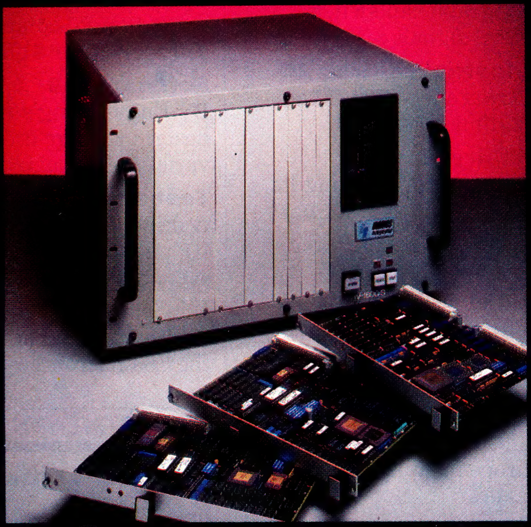

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PUBLISHER'S LETTER

TOGETHER AGAIN. Alex Wolfe, left, and John King as themselves.

The picture on the cover is a rather unusual introduction to two of our editors. Shown are equal parts of Alex Wolfe, whose right half is on the left, and John King, whose left half is on the right. They are graphically portraying the newly split market strategy at Silicon Compilers Inc.: to aim its second compiler system, introduced this week, at designers of integrated circuits, a smaller market than its first system, which was aimed at the relatively larger number of systems designers.

Adding to the seeming illogic of the new tactic is the fact that the first system, which was introduced a year ago, was designed to be used by systems designers precisely so they could avoid using the services of the IC folk. Why the company did this and what it hopes to accomplish are described in an article on p. 44, followed on p. 50 by an examination of the new system.

As for the cover models, news editor John King joined the *Electronics* staff in January. He is a native of Jersey City, N. J., who at 34 has studied and worked on both the East and West coasts. He received an English degree from St. Peter's College in Jersey City, then went to San Diego, where he wrote technical manuals for the Navy. While in California, he earned graduate credits at the University of Southern California and the University of California at San Diego. "I never thought I'd make the cover of a magazine," he says, "but at least they caught my good side."

Alex Wolfe, who was born and raised in the New York City borough of Queens, earned his BSEE in Manhattan at Cooper Union—after commuting to the Bronx for his studies at the renowned Bronx High School of Science. The 27-year-old spent five years in engineering—mostly designing software for the Lockheed P3B Orion, an antisubmarine-warfare aircraft—before joining the staff of *Electronics* in November 1984. Alex is now software & microsystems editor.

He doesn't see much difference between writing for a newsmagazine and writing the quick-working software that the military requires: "Basically, the difference is in the tools one uses."

The byline on the Sperry strike story (p. 21) contains a name new to the magazine. It is that of Gina G. John, a McGraw-Hill editorial trainee. Gina is working on *Electronics* as part of her internship—which entails three-month rotations among McGraw-Hill's weekly and monthly magazines and newsletters. A graduate of C. W. Post College, Gina has also completed an internship at the National Broadcasting Co.

Laurence Altman

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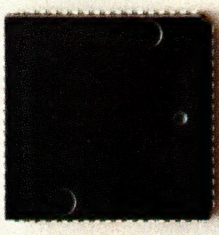

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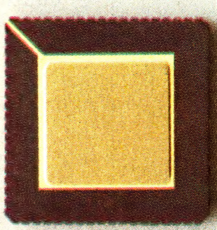

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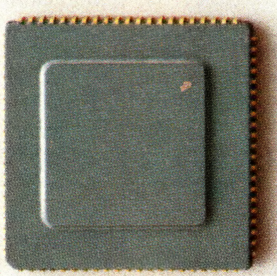

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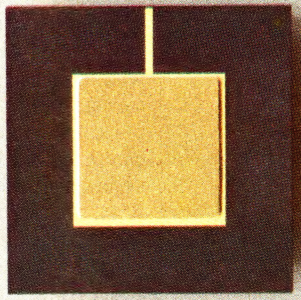

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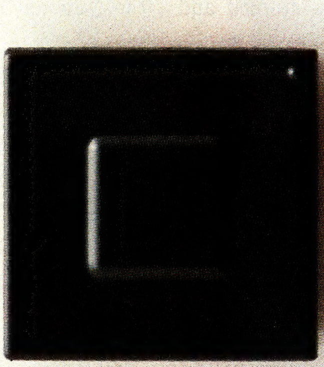

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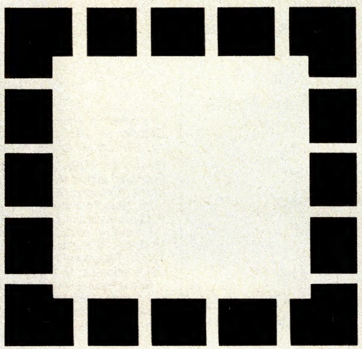

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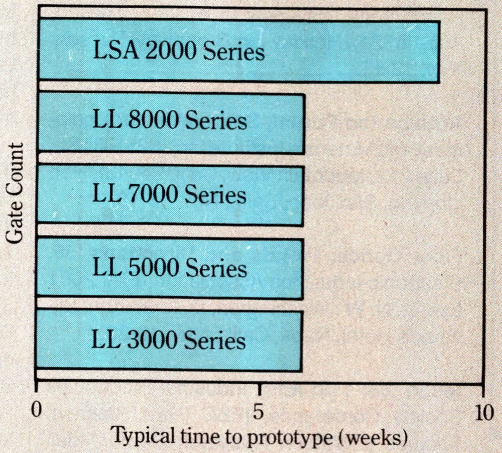

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MEETINGS

Artell '85: International Symposium on the Industrial Applications of Artificial Intelligence, Institute for Computer Engineering Research (Access Conference Associates Inc., P. O. Box 160, Gaithersburg, Md. 20877), Civic Center, Philadelphia, Nov. 5-7.

1985 GaAs IC Symposium, IEEE (James A. Hutchby, Technical Program Chairman, Research Triangle Institute, P. O. Box 12194, Research Triangle Park, N. C. 27709), Conference Center, Monterey, Calif., Nov. 12-14.

International Conference on Systems, Man and Cybernetics 1985, IEEE (Russ Ferrell, Systems and Industrial Engineering Department, University of Arizona, Tucson, Ariz. 85721), Holiday Inn-Broadway, Tucson, Nov. 12-15.

Automation Forum, Semiconductor Equipment and Materials Institute Inc. (625 Ellis St., Suite 212, Mountain View, Calif. 94043), Red Lion Inn, San Jose, Calif., Nov. 18-19.

Fiber Optics: Trends and Directions '85, Electronic Industries Association (EIA, 2001 Eye St. N. W., Washington, D. C. 20006), Silverado Hotel, Napa, Calif., Nov. 18-20.

Iecon '85: 11th IEEE Industrial Electronics Society Conference, IEEE (Ravi Prakash, Thomas J. Watson Research Center, Mail Stop 3-249, P. O. Box 218, Yorktown Heights, N. Y. 10598), Hyatt Regency, San Francisco, Nov. 18-22.

SCAE 1985, Society for Computer-Aided Engineering and American Fabricating Institute of Technology (Jan Dolman, Exposition Coordinator, American Fabricating Institute of Technology, 7811 N. Alpine Rd., Rockford, Ill. 61111), Astro Village Hotel Exhibition Center, Houston, Nov. 19-20.

ITC '85: International Test Conference, IEEE (ITC '85, P. O. Box 264, Mount Freedom, N. J. 07970), Marriott and Adam's Mark hotels, Philadelphia, Nov. 19-21.

Wescon '85, IEEE (Electronics Conventions Management Inc., 8110 Airport Blvd., Los Angeles, Calif. 90045), Moscone Convention Center, San Francisco, Nov. 19-22.

Conference on Factory Automation Models and Standards, National Bureau of Standards and U. S. Navy (U. S. Department of Commerce, National Bureau of Standards, Gaithersburg, Md. 20899), NBS Facility, Gaithersburg, Nov. 20-21.

Canadian Programmable Control Conference and Exhibition, IEEE (Kerrwil Publications Ltd., Trade Show Division, 501 Oakdale Rd., Downsview, Ontario, Canada M3N 1W7), Hamilton Convention Centre, Hamilton, Canada, Nov. 20-21.

Comdex/Fall '85, The Interface Group Inc. (300 First Ave., Needham, Mass. 02194), Convention Center *et al.*, Las Vegas, Nev., Nov. 20-24.

Scan-Tech Europe '85, Automatic Identification Manufacturers Inc. (AIM, 1326 Freeport Rd., Pittsburgh, Pa. 15238), Jaarbeurs Congress & Exhibition Centre, Urtrecht, the Netherlands, Nov. 25-28.

Infocoms, RAI Gebouw and Industrial Presentations (Europe) (Amsterdam RAI, Europaplein, Amsterdam, the Netherlands), RAI Exhibition Centre, Amsterdam, Nov. 26-29.

International Test and Measurement Exhibition and Conference '85, Network Events Ltd. (Printers Mews, Market Hill, Buckingham, MK18 1JX, England), Olympia 2, London, Nov. 27-29.

IEDM: 31st International Electron Devices Meeting, IEEE (Electron Devices Society of the IEEE, 655 15th St. N. W., Suite 300, Washington, D. C. 20005), Washington Hilton and Towers Hotel, Washington, Dec. 1-4.

Globecom '85: IEEE Global Telecommunications Conference, IEEE (G. A. Ledbetter, South Central Bell, 365 Canal St., New Orleans, La. 70140) Hyatt Regency, New Orleans, Dec. 2-5.

Materials Research Society Fall Meeting, Materials Research Society (9800 McKnight Rd., Suite 327, Pittsburgh, Pa. 15237), Marriott Hotel at Copley Place, Boston, Dec. 2-6.

1985 Power Semiconductor Devices Workshop, IEEE and National Bureau of Standards (Sandra B. Kelley, NBS, Bldg. 225, Rm. B3444, Gaithersburg, Md. 20899), NBS, Washington, Dec. 5.

WSC '85: Winter Simulation Conference, IEEE *et al.* (Gerard C. Blais, U. S. Air Force, Washington, D. C. 20330), Hilton and Tower Hotel, San Francisco, Dec. 11-13.

CAIA: Second Conference on Artificial Intelligence Applications, IEEE (Artificial Intelligence, P. O. Box 639, Silver Spring, Md. 20901), Fontainebleau Hotel, Miami Beach, Fla., Dec. 11-13.

Winter National Design Engineering Show & Conference, American Society of Mechanical Engineers (Cahners Exposition Group Inc., 999 Summer St., Stamford, Conn. 06905), Convention Center, Anaheim, Calif., Dec. 11-13.

1st International Conference on Supercomputing Systems, IEEE (Supercomputing Conference, P. O. Box 639, Silver Spring, Md. 20901), Innisbrook Resort, Tarpon Springs, Fla., Dec. 16-20.

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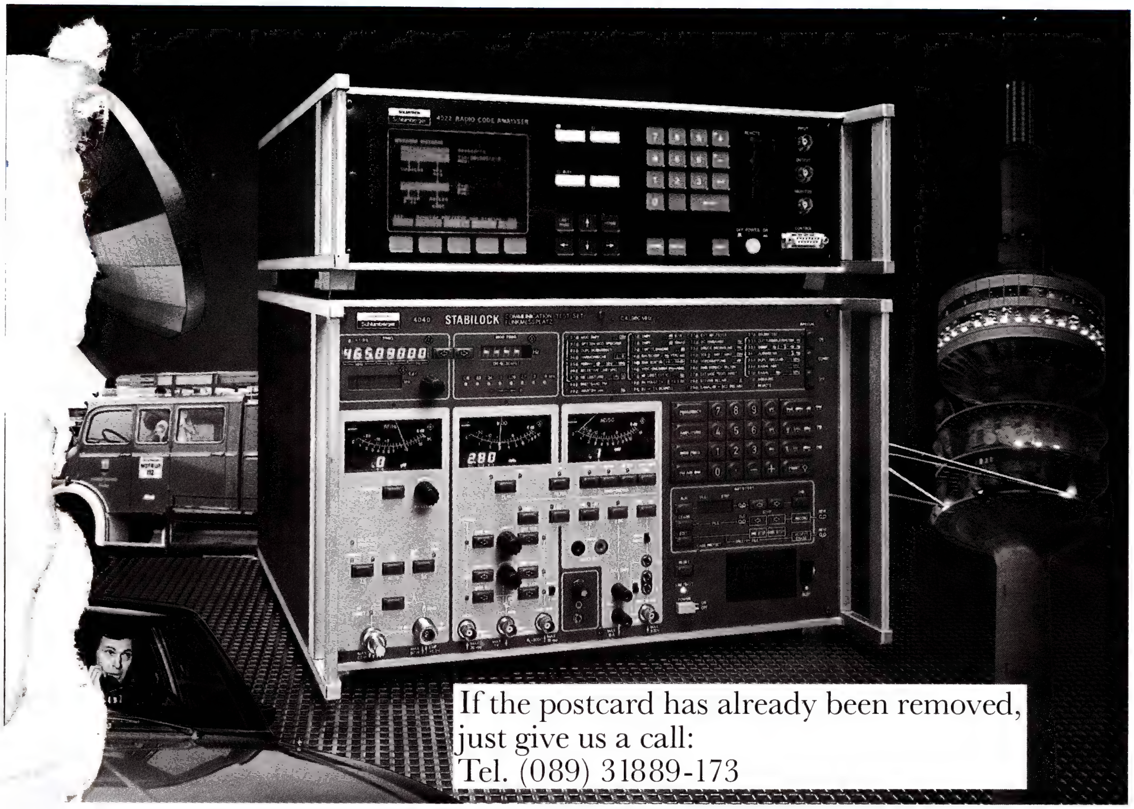

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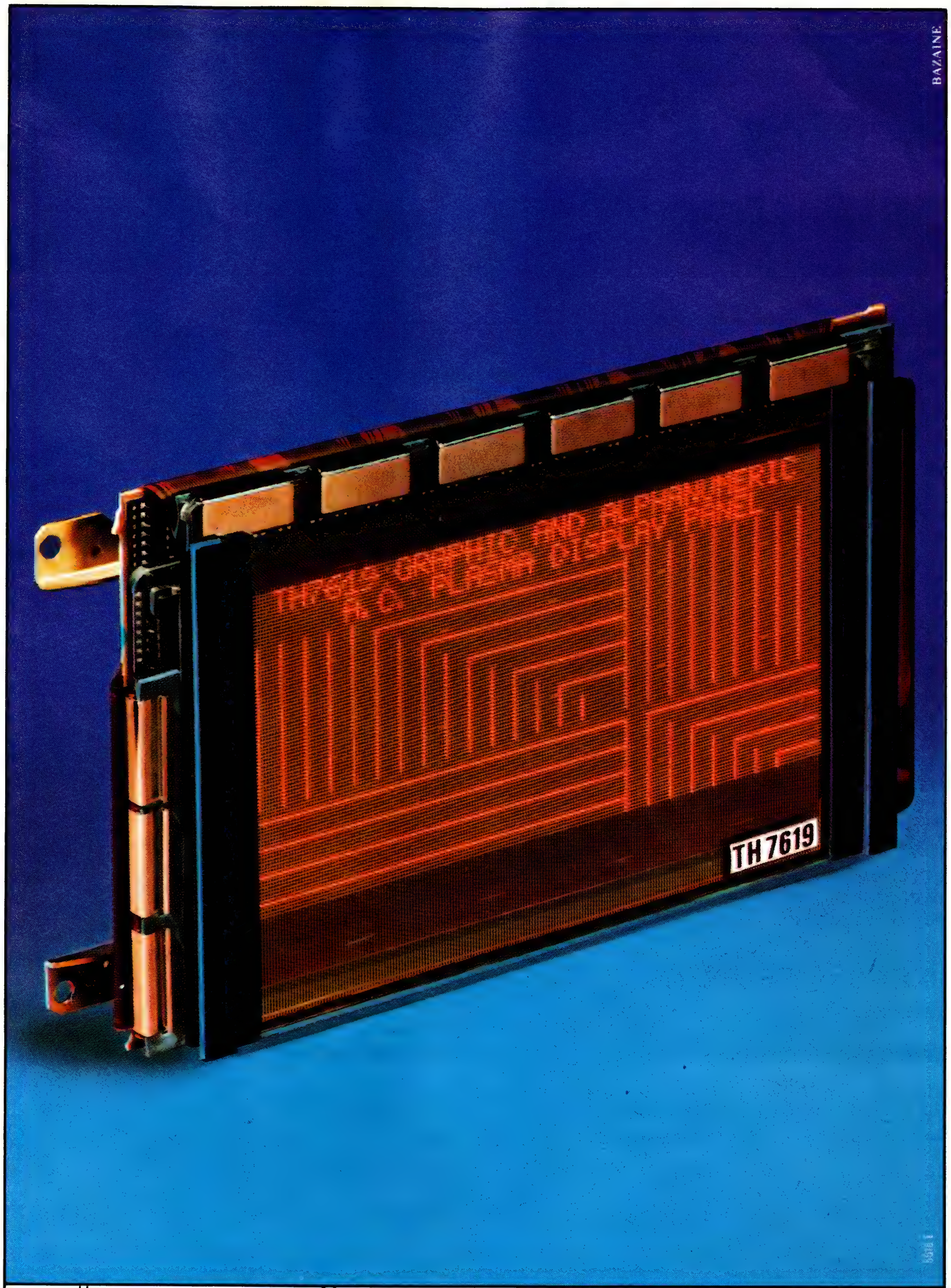

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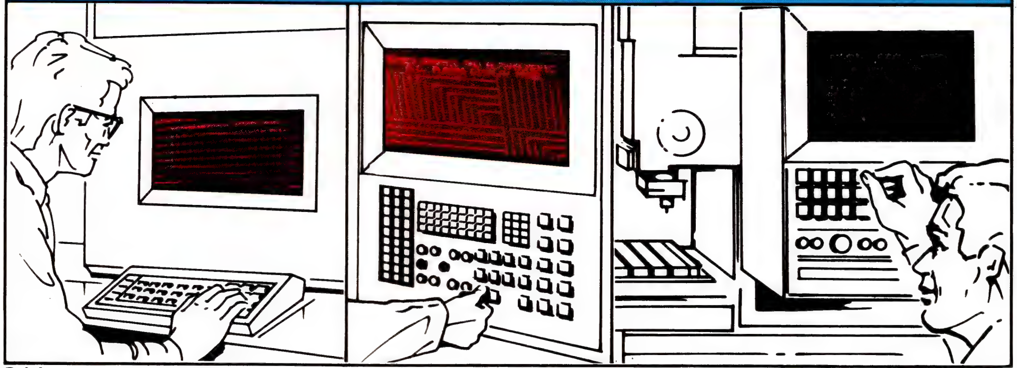

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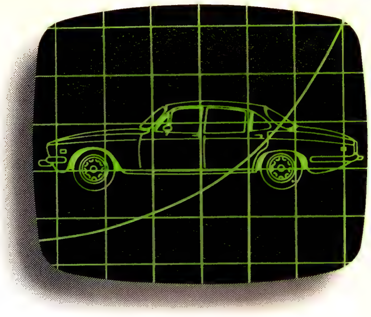
Position Sensing Devices For Automotive Electronics



A Collaborative Effort.

It's not unusual to find all types of new electronic devices in the automobile today. While many are IC's and microprocessors, flexible circuitry, displays and controls, the emergence of position devices opens new, practical avenues for answering the challenges of accurate feedback.

At Duncan Electronics, for example, a host of applications is being answered through early relationships with customer design and manufacturing engineers. The result is greater assurance of exact fit, performance and realistic cost. In fact, while many electronic or mechanical sensing device requirements may initially suggest unique design, customers have often discovered their problems have already been solved.

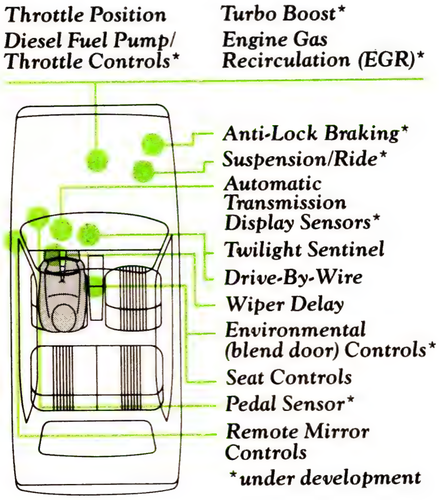
Throttle Position to Remote Mirror Controls.

Today, an expanding family of standard products have risen from these unusual packaging requirements, opening even more cost effective possibilities. Developed initially for throttle position sensing, a resistive element, configured on a special shaped substrate for interface with an existing mount, is performing reliably in millions of vehicles on the road today.

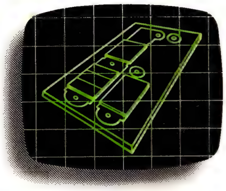
Most recently, a special module designed for harsh under-hood environments led to the introduction of Duncan's 9800 Series. It is now available in twelve standard configurations, ideal for throttle position sensing and other feedback applications.

With slight modification in packaging to the popular 9600 Series linear motion sensors, Duncan developed a miniaturized X-Y axis control/positioning device for remote rear-view mirrors. These compact devices provide ±2% to 0.35% linearity in ½″ to 1½″ electrical strokes.

Automotive transmission sensor functions are answered with Duncan's series 98E resistive elements. Passenger seat location, wiper delays and cruise controls are only a few of the "on-board" applications that have been cost-effectively answered. And applications such as EGR, environmental control "blend doors," anti-lock braking and suspension/ride sensors are under development. Devices featuring reliability and miniaturization are the result of a collaborative effort between sensor maker and sensing needs.



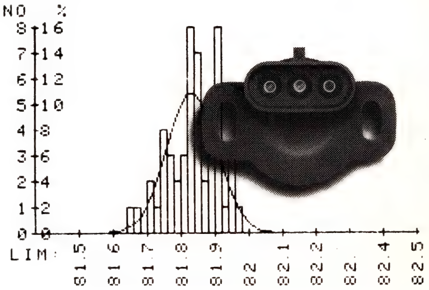
Statistical Process Control



Comprehensive statistical process control must be employed in the manufacturing process. It means you can be confident of consistent quality and reliability from high-volume production. At Duncan, this process is aided by computer-based in-process controls to facilitate the immediate and accurate identification of problems and trends. Corrective measures are taken before parts are produced, to assure the highest possible yield of extremely dependable products.

Prototype testing and sampling programs, prior to volume production, provide added assurance of "in-system" performance of all Duncan automotive products. Process capability studies provide capability ratios with sample size, mean averages and related statistics. Another step includes automated and semi-automated testing techniques which monitor all manufacturing steps via computer-controlled test stations.

A direct benefit is the ability to provide uniformly reliable products at lower cost while allowing the user to eliminate costly incoming inspection procedures.



Design Primer

Ask for a free copy of Duncan's PRIMER OF POSITION SENSING DEVICE DESIGN FOR AUTOMOTIVE ELECTRONICS and complete data on standard position sensing products. You can realize new applications for position sensing by sharing your requirements with your Automotive Electronics colleague. Write to Duncan Electronics, 2865 Fairview Road, Costa Mesa, CA 92626. Or, for immediate response, call (714) 545-8261 and request your copy today.
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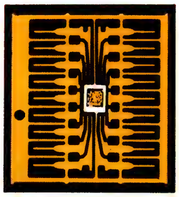

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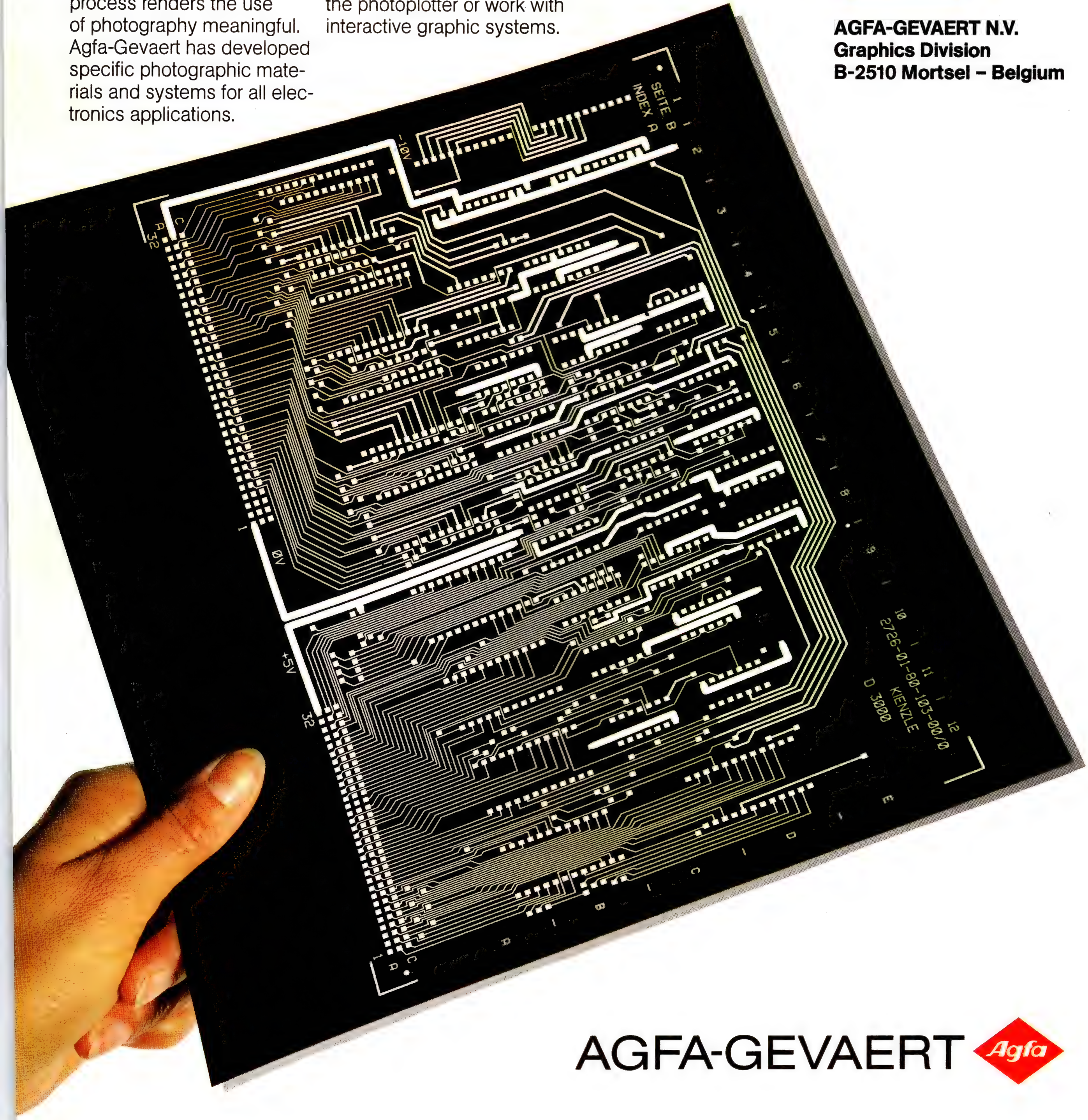

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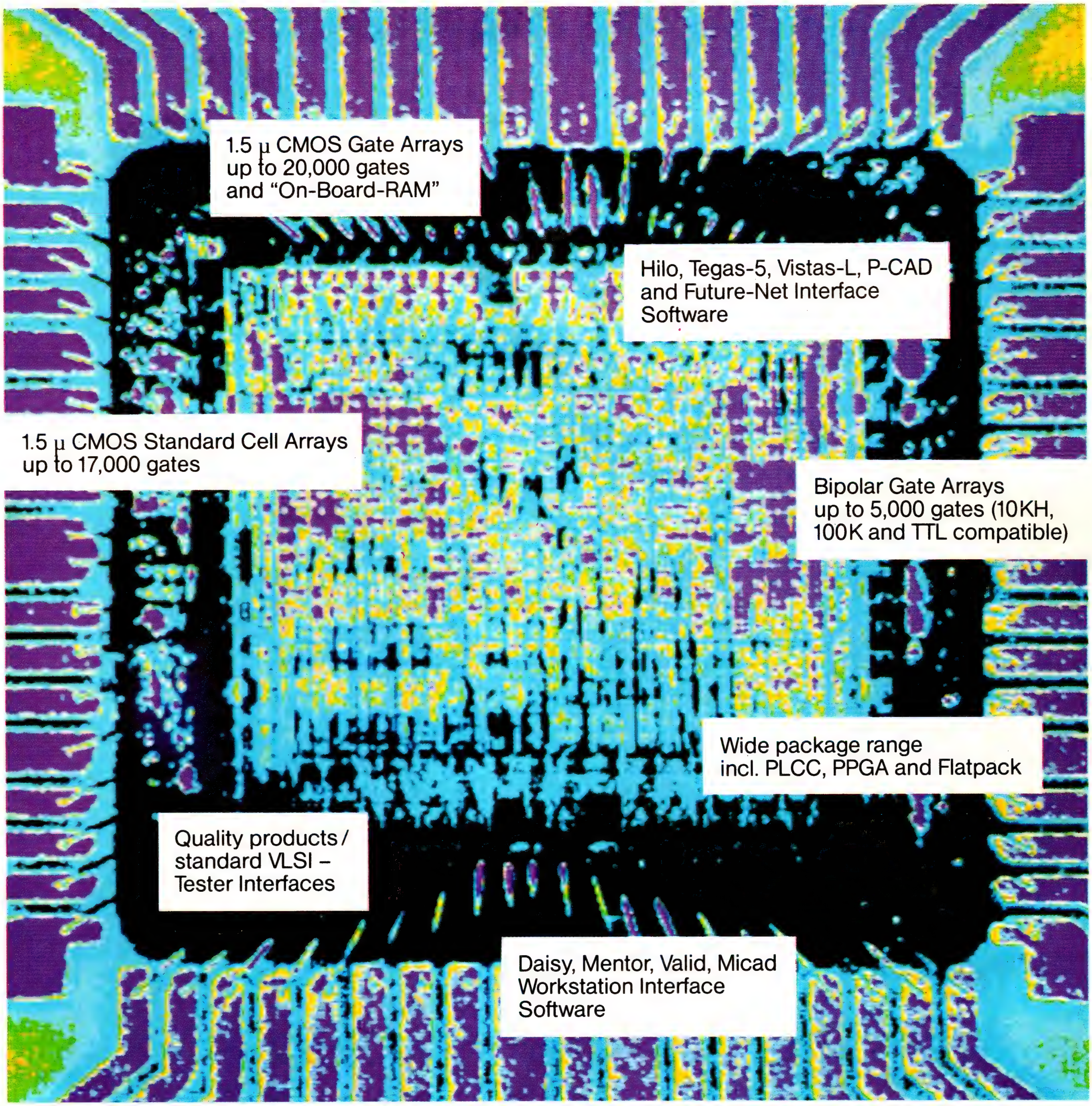

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ELECTRONICS NEWSLETTER

INTEL HOPES 80386 CHIP WILL CATAPULT IT TO 32-BIT PROMINENCE

Although Intel Corp. has been late in bringing out a 32-bit microprocessor, it hopes to leapfrog the field when it introduces its 80386 megachip this week. Alone among available 32-bit processors, the 386 supports both the MS-DOS and Unix operating systems, allowing simultaneous use of software written for either one. With this feature, plus compatibility with all existing 8086-family software, Intel hopes to sell its chip into both the office and high-end work-station markets. The Santa Clara, Calif., chip maker claims performance of 3 million to 4 million instructions per second for the 386. The chip measures almost exactly 1 cm^2, can address 64 trillion bytes of virtual memory, and performs all memory management itself. Intel only recently began sampling the chip, yet it already reports some design wins. □

EIA SAYS DEFENSE SPENDING WILL DROP, BUT ELECTRONICS IS UP

Defense spending will decline 3.1% by 1995, although the electronics portion of the defense budget will increase by 3.2%. That's the latest prognosis from the Electronic Industries Association. The EIA was the first to predict that an upswing in defense spending would end by the mid-1980s. Now it says defense spending on electronic goods and research will go from $54.3 billion in 1985 to $56.5 billion in 1986 and $58 billion in 1995. Increases in electronics spending stem largely from the Strategic Defense Initiative program. Ironically, perhaps, the EIA also says that the White House will not get nearly what it wants for SDI over the next 10 years; in fact, it predicts that this year's request for $3.86 billion will result in congressional approval of $2.5 billion. □

IN-STAT SEES ANOTHER DOWN YEAR

The semiconductor market will be down 3.3% in the U. S. next year, according to the latest forecast from In-Stat Inc., Scottsdale, Ariz. Markets in Japan and Europe will also drop, by 3% to 5%, according to the market research company. In-Stat says limited growth will come from the rest of the world, which includes Korea and Australia. For the U. S. market, the forecast sees pricing pressure in a general economic recession in 1986 driving semiconductor dollar volume down 3.3% while actual unit sales remain flat. The company predicts the U. S. market will be down a total of about 30% this year, at the $6.6 billion level, compared with last year's $9.7 billion. The light at the end of the tunnel will come in 1987, with a jump of 19% in U. S. sales; 1988 is expected to be even better, with 28% growth. □

VCRs, COLOR TVs RACKING UP BANNER SALES YEAR

Sales of video cassette recorders continue to climb at a dizzying rate despite consumer confusion over the benefits of the new 8-mm format. Figures released last week by the Electronic Industries Association's Consumer Electronics Group show that factory sales to U. S. dealers of 7.5 million units during the first three quarters this year nearly equaled the total 7.6 million VCRs sold during all of 1984. Compared with the same period last year, that's a 57% jump, and the group this May predicted a 51% increase for the year to 11.5 million units [*ElectronicsWeek*, June 10, 1985, p. 14]. Color TV sales are also posting gains, following a record year of 16.1 million units moved in 1984. September color TV shipments jumped by 10.5% compared with the same month last year, bringing the nine-month total to 11.6 million units. Among other video categories, projection TV sales were up by 27.8%—to 161,000 units—for the first nine months. Color video cameras and monochrome TV sales, though, were off by 4% and 26.4%, respectively. □

ELECTRONICS NEWSLETTER

MEASUREX AND FORD MOVE INTO DISCRETE CIM MARKET

Measurex Corp., in a deal with the second-largest U. S. automaker, is adapting its continuous-process computer-integrated-manufacturing system to a discrete factory operation, in which parts are made separately and then assembled. With this move, Measurex is taking aim at a market it projects at $5.4 billion annually in 1990. Ford Motor Co. will match the $7.2 million Measurex is putting up over three years to develop CIM software modules for Measurex's Vision 2002 network. The network combines automated procedures with a materials and accounting data base. The Cupertino, Calif., company has been selling Vision 2002 since 1983 to metals, plastics, and chemical manufacturers for continuous-process applications, in which one complete product is manufactured. Ford plans pilot programs in discrete applications for its Woodhaven, Mich., stamping plant and its Wayne, Mich., assembly plant. It will use the Manufacturing Automation Protocol to link individual islands of automation. ☐

AEA OPPOSES HOUSE TAX-REFORM PROPOSAL

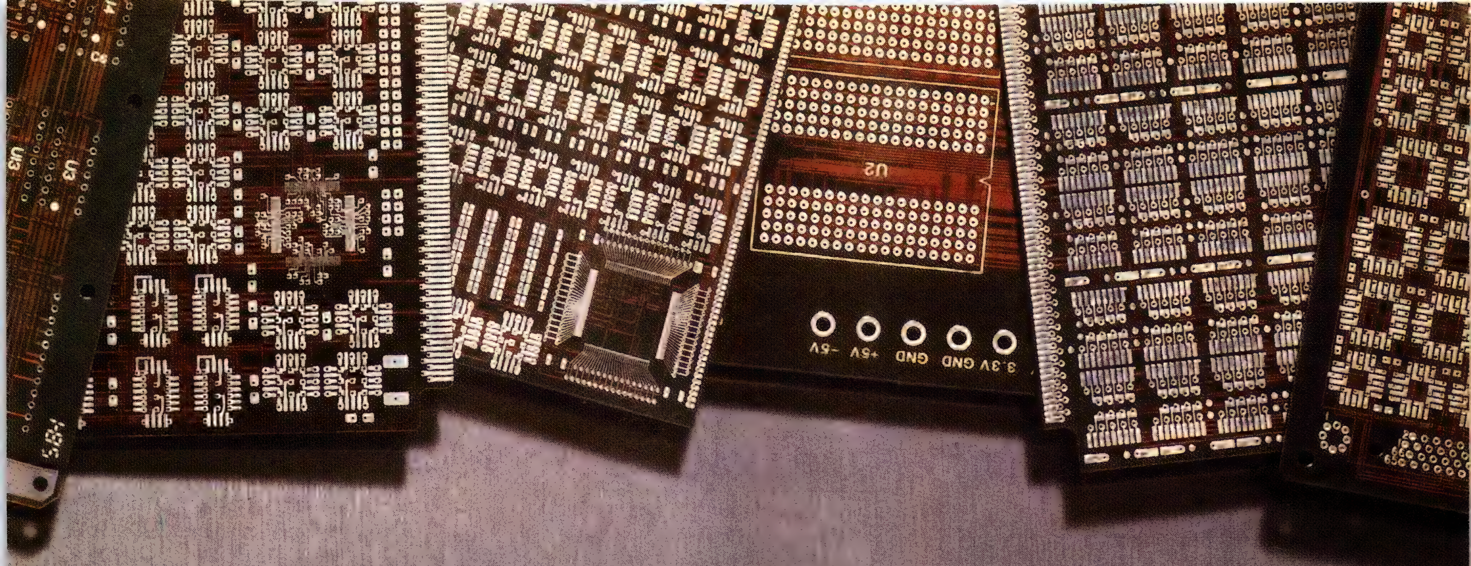
American Electronics Association chairman William G. Moore promises to apply a "full-court press" to block a House Ways and Means Committee's proposal to cut the research and development tax credit by at least 75%. Last week, the AEA began intense lobbying efforts aimed at preserving intact the R&D tax credit and eliminating other proposed taxes. These efforts come in response to the House committee's redraft of the Reagan Administration's Treasury II tax-reform proposal announced in May [*ElectronicsWeek*, June 3, 1985, p. 13]."We're lobbying for nothing less than the return of the original Treasury II (R&D) tax credit," says Moore. Treasury II would extend the tax credit three years. AEA's Kenneth Hagerty says 22 of the 36 committee members would sponsor a bill to make the credit permanent. ☐

FCC AGAIN RULES AGAINST NON-WIRELINE CELLULAR CARRIERS

Another non-wireline cellular telephone carrier has come up empty at the Federal Communications Commission. Florida Cellular Telephone Co., Miami, had argued that all cellular customer equipment should include a device that lets subscribers select operation on frequency block A or B on the theory that one setting could be used for Bell South Mobility Inc., the local Bell operating company, and the other for a non-wireline carrier. Florida Cellular claimed that a switching device would balance the competitive advantage inherent in Bell South's head start. The FCC, however, reasoned that selection of a non-wireline carrier would require reprogramming of the telephone, regardless of the existence of an A/B switch. The FCC has denied anticompetition petitions against BOCs by nearly 30 non-wireline carriers. ☐

TWO-YEAR-OLD POWER-SEMICONDUCTOR COMPANY FILES CHAPTER 11

Texet Corp., a power-semiconductor startup north of Dallas, has entered a new chapter in its young history. Unfortunately for Texet, it was Chapter 11. Backed originally by a group of French investors, Texet was launched in 1983 to carve out a niche in smart power [*Electronics,* June 30, 1983, p. 53]. However, the market boom of 1983 sidetracked the startup into older bipolar discrete power units, causing a delay in the introduction of MOS FET smart-power units made from its Trimos triangular-cell technology. Forty-nine of the 85 employees in Allen, Texas, have been furloughed for two weeks. Also, Texet's assembly-test plant in Ste. Michele-sur-Meurthe, in eastern France, has been placed under a provisional administrator by the French government and will likely be sold. ☐



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Electronics

SUPERDENSE MEMORY DEVICES ARE EVOLVING FROM BUBBLES

THE WALL AROUND EACH BUBBLE WILL STORE ABOUT 100 BITS

RYE BROOK, N. Y.

When traditional magnetic disks and the upcoming magneto-optic drives run out of steam, yet another magnetic-storage technology—Bloch-line memory, a descendant of magnetic-bubble memory—may be ready to take over. The technology promises densities on the order of a few gigabits per square inch, as well as very fast parallel-associative searches of vast data bases.

"Bloch-line memory technology is one of the most dense memory structures yet seriously considered—denser than bubbles and magneto-optic disks," according to Mark H. Kryder of the Magnetics Technology Center at Carnegie-Mellon University. Kryder presented a report on the new technology at last week's International Conference on Computer Design in Rye Brook held by the IEEE, where Bloch-line memory sparked considerable interest.

The Bloch-line memory concept uses a magnetic domain—very much like a conventional bubble—in the form of a stripe. The stripe is an elongated segment within a thin-film bubble-memory material (figure, part a). The polarity of the stripe region's magnetization is reversed with respect to the surrounding material's polarity. Through the finite transition layer (domain wall) separating the oppositely polarized regions, the magnetization rotates gradually from one orientation to another rather than in an abrupt discontinuity (figure, part b).

The magnetization in the wall can twist either clockwise or counterclockwise so that in the center of the wall, the magnetization points either one way or the other. Regions running from the top to the bottom surfaces of the film separate the clockwise-twisting segments from the counterclockwise ones. These regions are called Bloch lines and are indicated by the red upward- and downward-pointing arrows within the domain wall.

Two adjacent Bloch lines, a stable combination, are used to represent a 1 bit; an absence of Bloch lines represents a 0. The distance between Bloch lines is short, so many bits can be stored in the wall of one stripe, giving the technology its prospects for very high bit density. In a bubble memory, one bubble domain represents one bit; but in Bloch-line technology, a small stripe about 0.5 µm wide may carry up to 100 bits.

Bloch-line technology will pack gigabits in one square inch

Bloch-line memories will eventually be produced using techniques similar to those for making bubble memories. The stripes are organized in major and minor loops, as are conventional bubble memories. Bits stored as Bloch lines in the domain wall of one stripe circulate in shift-register fashion—a minor loop. Many stripes together form the major loops, which move the data to and from the chip's input/output structures. The I/O structures are similar to those used in bubble-memory technology.

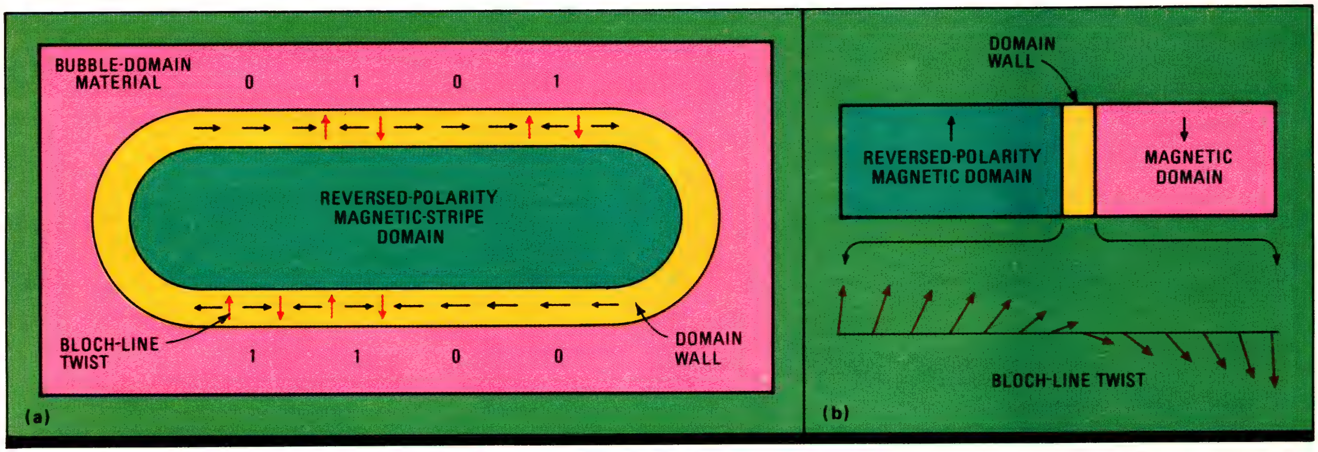
The bits are read at one end of the stripe and generated (written) at the other end. A read operation converts Bloch lines into bubbles, and writing converts bubbles into Bloch lines.

HIGH-SPEED ACCESS. The stripe structure of Bloch-line memory, plus the possibility of putting logic on the chips, offers a tremendous parallel-access opportunity. Thus extremely fast associative data searches will be possible with this technology, according to Kryder. It may be possible to search through 1 gigabyte in as little as 0.01 second, he says.

Researchers at Carnegie-Mellon have made write gates to verify the principles for writing Bloch lines. They have also shown how to interface a Bloch-line stripe with a bubble stream to get the information into the memory.

It appears that another technology race is on between Japan and the U. S. In what may well be a race for the next dominant mass-storage technology, the U. S. is already behind, at least in research funding.

In addition to work at Carnegie-Mellon and Purdue University, Bloch-line



RACEWAY. Within the wall that divides an elongated magnetic bubble from the oppositely polarized area around it (a), 100 or so bits can be stored as Bloch lines. A Bloch line is a point where the field twist from the wall's inside to its outside (b) changes its direction of rotation.

technology is getting serious scrutiny in Japan at NEC Corp. and Kyushu University. Research is under way as well at the Universität-GH Wuppertal in West Germany.

Pioneering research work on the dynamics of the walls surrounding magnetic domains in bubble memories by Floyd B. Humphrey, principal research scientist at Carnegie-Mellon, is the basis for the original memory-technology proposal made by Kyushu University's S. Konishi and NEC's Y. Hidaka and K. Matsuyama in papers presented at the MAG-19 magnetics conference in 1983. In this proposal to turn Humphrey's research to practical use, the Japanese researchers claimed a limiting density of 200 megabytes/cm^2.

Since the 1983 conference, Humphrey and others at Carnegie-Mellon have also been working on practical memory devices. But the U. S. efforts have nothing like the funding that Konishi and company have—$1 million, claims Humphrey. "The Japanese are going full-bore on this," he says. Bloch-line memory devices may make it to the product stage in five to seven years, Humphrey and Kryder predict.

Konishi has formulated an idea and demonstrated the practicality of the physics for detecting (reading) a Bloch line. The Carnegie-Mellon researchers are in the process of making the masks to show the practicality of Konishi's reading concept. This leaves a lot of work to be done in developing the technology to realize its density potential, test the medium's stability, and develop a manufacturing process.

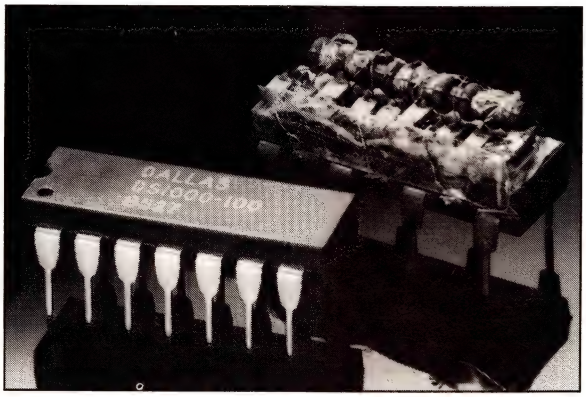
A year ago, Humphrey thought Bloch-line memory technology was about 10 years away from product reality. Now, after considering the Carnegie-Mellon group's progress over the past year, he has shortened that projection by at least three years. *–Tom Manuel*

SEMICONDUCTORS

LASER-SELECTED OPTIONS SET CHIP UP FOR NICHES

DALLAS

Laser beams could help divine yet another semiconductor market, wedged between the huge commodity-chip business and the emerging semicustom arena. Next week, Dallas Semiconductor Corp. will take aim at this potential market, introducing its first late-definition components tailored by direct write of lasers. In this approach, patterns and options are written into the silicon of fabricated chips when they are still on wafers. Then the chips are cut apart and packaged.



CLEAN CUT. Lasers set the timing on Dallas Semiconductor's delay-line IC, which replaces hybrids like the one behind it.

For its first offerings, the 1½-year-old company is using highly accurate laser systems to set timing parameters of new monolithic silicon delay-line circuits. But beyond the initial application of its laser technique, Dallas Semiconductor believes a whole new chip market is waiting: high-volume integrated circuits that can serve smaller niches by offering laser-selectable options.

"This is a way of making standard products cover a greater application range than would otherwise be possible," says Michael Bolan, marketing director and one of the company founders who left Mostek Corp. in order to pursue new late-definition chip technologies [*ElectronicsWeek,* Jan. 7, 1985, p. 17]. "Unlike firms promoting user-designed semicustom ICs, we have a philosophy that there will be something between standard and semicustom products. We think it will be standard products that have 'optioning' capability, and optioning will be brought about by lasers."

A way to make standard products do more

The company says its new CMOS chips are the first significant advance in two decades for delay-line components. Delay-line devices, which have remained hand-made hybrids since they first appeared in the 1960s, are used widely to synchronize memory data. The new monolithic DS1000 silicon delay lines are potentially lower in cost than the hybrids, vary by only 1 ns over a wide temperature range, and can be surface mounted.

Initially, Dallas Semiconductor will use advanced lasers based on a neodymium yttrium-aluminum-garnet compound on half a dozen products. In addition to setting the timing characteristics of its 14-pin delay-line chips, the company will use Nd:YAG lasers to program in options on telecommunication circuits and create unique features for a new line of secure-memory software cartridges.

Lasers are used in an isolated area of the chip, separated by guard rings from circuits that would be damaged by the blast. Options can be chosen by selectively blowing fuses—a process normally used for correcting chip faults. Security and timing parameters are created by writing patterns on special targeted areas of the fabricated die. With this nontrimming technique, the laser beam creates a certain code word by writing nonvolatile bits into the silicon. These bits define a calibration constant, and the code word changes the definition of the part. The laser equipment, made by Quantronix Corp. of Smithtown, N. Y., can position the beam to 1-μm accuracy.

With the DS1000 delay lines, the laser system automatically positions each silicon die before writing a patterned calibration constant. Dallas Semiconductor has developed a number of proprietary positioning and laser-control programs for the equipment, which uses pattern recognition to align targets. The patterns on the 7,500-mil^2 delay-line chip will set timing characteristics to within 1 ns of any speed chosen. The laser-programming systems are being set up to handle tens of millions of silicon delay lines next year.

EXPEDITIOUS. Bolan says laser-programmed options not only will serve customers better, but also will help expedite chip introductions by as much as two years because engineers can complete product definition without waiting for market standards to emerge fully.

"Telecom is a particularly good example of an area where much of the time is spent in product definition. It's a real moving target," he notes. "Now, if we know what 90% of the chips will be, we can complete the design. The remaining 10% can be set by laser after chips are fabricated." Dallas Semiconductor will use the option-tailoring approach on a new 40-pin serial T-1 transceiver.

The direct-write laser work is the second tine of Dallas Semiconductor's three-pronged thrust into new methods for low-cost application-specific ICs and to date involves the most heavily researched technology. This year, the company introduced 14 IC products featuring nonvolatile memories backed by embedded lithium energy cells. Customers and makers of end equipment can set chip features by loading software into lithium-backed memory. Next year, the company plans to start using a high-voltage ion-implantation technique to customize entire completed wafers for express delivery of chips.

The young company considers the introduction of its new laser-programmed chips a critical step. "We are betting a major portion of the company on the laser technology," admits Bolan. A half dozen U. S. patent applications stem from the 14-pin silicon delay line. Three of the patent applications cover circuit-design techniques—one involves topology, and two are for laser-processing techniques. *–J. Robert Lineback*

LOCAL-AREA NETWORKS

NEW SNA PROTOCOLS LOOK TAILORED FOR TOKEN RING

SAN JOSE, CALIF.

The curtain is about to fall on the first act of IBM Corp.'s token-ring-network drama. Industry sources indicate that price and availability of IBM's long-awaited token-ring local-area network will be announced this week, or very shortly thereafter.

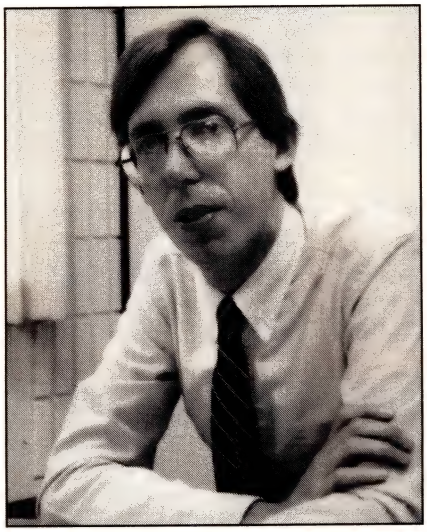
Once details of the token ring's physical connection and data-link-layer network-management functions are revealed to end the first act, the curtain is sure to come up on another scene—the one that depicts how the token ring fits into the Systems Network Architecture, IBM's master networking plan.

IBM has been systematically leaking details of an adjunct to SNA dubbed Low Entry Networking, whose protocols appear appropriate for use on a token ring. Analysts familiar with the computer giant's network plans say SNA/LEN makes it almost as easy to change the logical structure of the net as the token-ring connection makes moving devices around, so they expect some SNA/LEN details to be unveiled at the ring announcement.

PEER TO PEER. SNA/LEN revamps the mainframe orientation of SNA with peer-to-peer communication and dynamic-reconfiguration capabilities. For example, under SNA/LEN, two intelligent devices such as engineering work stations can communicate directly across the net without a mainframe intermediary. And if one is moved to a new location, SNA/LEN greatly simplifies updating network routing tables and directories.

Communication will not require a mainframe

Because the IBM local network is implemented as a superset of the Institute of Electrical and Electronics Engineers' 802.5 token-ring standard, non-IBM devices with an 802.5 interface will be able to make the physical connection and share the same cable. However, analysts caution that such devices will be doing without the diagnostic and network-management capabilities IBM is building into its interface. Non-IBM interfaces will not have the hooks necessary to take advantage of SNA/LEN.



NET WATCHER. LEN protocols will bring dynamic reconfiguration to the SNA world, says Communication Solutions Inc.'s Czubeck.

One of the biggest criticisms leveled at SNA is that network addressing and routing tables must be set up in advance. This means that every time a device is wheeled across the floor, the entire network must be brought down and the network addressing and routing tables modified—usually by a large support staff—before it is brought up again.

What has been missing is the ability to reconfigure the network dynamically, says Donald H. Czubeck, vice president of technical development for Communication Solutions Inc., San Jose, Calif. The company, which is owned by Control Data Corp., specializes in IBM-compatible data communications.

Over the last several years, IBM has been quietly introducing office-automation products that support peer-to-peer communications through SNA enhancements called Logical Unit 6.2 and Physical Unit 2.1, says Czubeck. The enhancements let network nodes communicate directly and handle multiple communication sessions. Most notable among the products with these enhancements have been the System/38 Display Writer and the System/36 Departmental Processor.

SNA/LEN modifies both Logical Unit 6.2 and Physical Unit 2.1, adding the ability for a small-system node to take care of routing for sessions not intended for itself. Furthermore, the small-system node will act just like a full network node, since it will have full knowledge of the network's topology.

"SNA/LEN sets the stage for the migration of network technology," Czubek explains. "What it adds is the ability to move or add a work station to a network and have those work stations dynamically distribute their addresses to all the other stations in the net."

DIAGNOSTICS. Though SNA/LEN will greatly increase the distribution of intelligence across the network, a mainframe computer will continue to handle the crucial role of network management and diagnostics, Czubeck says.

There are two major mainframe programs dedicated to network management and diagnostics. One is for diagnosis of the physical network—such problems as modem failures, data-link failures, and noisy communication lines. The other takes care of diagnostics in the logical net and the higher levels of SNA protocols; its main job is fixing errors made in configuring the net and detecting SNA protocol errors.

The two SNA diagnostic packages use information sent to the mainframe by the IBM token-ring adapter boards on the network. This data is not available from other 802.5-interface products. Without the diagnostics of SNA's mainframe software or the dynamic configurability afforded by LEN, non-IBM devices with 802.5 interfaces will be able to share the physical connection, but little else. *–Robert Rosenberg*

PERSONAL COMPUTERS

AT&T ADDS MUSCLE TO BATTLE IBM

NEW YORK

Adding more ammunition in its battle with IBM Corp. for the hearts and minds of corporate America, AT&T Co.'s Information Systems Division last week displayed powerful additions to its personal computer line, the most prominent being a version of IBM's Personal Computer AT that runs programs simultaneously under the Unix and MS-DOS operating systems.

Industry analysts note that AT&T's

addition of a PC AT look-alike merely satisfies one requirement to do business in the personal computer market. But the bridge AT&T now offers between MS-DOS, the most popular personal computer operating system, and Unix, AT&T's bread-and-butter operating system, could strengthen AT&T's market position significantly.

"AT&T's entire strategy is based on Unix," notes George Colony, president of Forrester Research Inc., Cambridge, Mass. "They need some way to civilize Unix. The product attempts to do that."

OUTDONE. "We have out-PC-AT'ed IBM right now," said a jubilant James D. Edwards, president of AT&T Computer Systems Division, Morristown, N.J., in announcing the new products. "The ability to run DOS and Unix separately and together [on the same machine] frees customers from the necessity to choose between DOS and Unix" when buying a personal computer.

AT&T's new personal computer is the PC 6300 Plus, made for it by Ing. C. Olivetti & C. Like the PC AT, it uses Intel Corp.'s 80286 microprocessor. AT&T says the computer is designed without wait states, so it runs 25% faster than the PC AT. Like the PC AT, the 6300 Plus costs $6,320 for a standard configuration that includes 512-K bytes of main memory, a 1.2-megabyte floppy disk, a 20-megabyte hard disk, monitor, keyboard, and serial and parallel ports.

Available immediately, the 6300 Plus is "100% hardware- and software-compatible with the IBM PC/XT, unlike the PC AT," Edwards pointed out. A kit to upgrade older 6300 machines to the new 6300 Plus will be available in December for $2,995. Industry analysts estimate 10% to 15% of the users of the older 6300 will buy the upgrade kit. Colony of Forrester Research expects AT&T to ship 95,000 of the PC 6300s in 1985, bringing its installed base by the end of this year to 110,000 machines.

AT&T's bridge to MS-DOS could civilize Unix

AT&T will have available in the first quarter of 1986 a $375 software package called Unix/OS Merge. This will allow 6300 Plus users to run programs written for the MS-DOS operating system at the same time they're running programs written in Unix. With the package, MS-DOS runs as a Unix task, allowing "full multitasking in the DOS environment," Edwards added.

To upgrade its Unix machine, also known as the model 7300, AT&T introduced the DOS-73, a $995 coprocessor board made by Alloy Computer Products Inc., Framingham, Mass. Containing an Intel 8086-2 processor with half a megabyte of random-access memory, the DOS-73 board allows a model 7300 to run MS-DOS version 3.1 "at a considerably higher speed than that of an IBM PC/XT," AT&T said. As a result, the 7300 with DOS-73 can run popular MS-DOS software packages, such as Lotus Development Corp.'s 1-2-3 integrated spreadsheet, for the first time. The 7300 is made for AT&T by Convergent Technologies Inc., Santa Clara, Calif.

Taking aim at IBM's System 36/PC, AT&T introduced the Unix PC model 3B1, which Edwards called "a bridge system between the minicomputer world and the personal computer world." The machine, based on Motorola Corp.'s 68010 microprocessor, will be available next month at prices ranging from $8,495 to $9,995, depending on which of the three configurations chosen. Optimized for five users (though it can handle up to nine), it "sets a new standard for price performance," Edwards said.

The new 3B2/310 machine can handle up to 14 users, Edwards said, which puts it between the 10-user 3B2/300 and the 25-user 3B2/400 products. An optional math-acceleration coprocessor gives the 3B2/310 "MicroVax II-like performance," according to Edwards. Prices for the 3B2/310 range from $13,950 to $18,900. *–Robert J. Kozma*

OPTOELECTRONICS

HOLOGRAPH SWITCHES OPTICAL SIGNALS

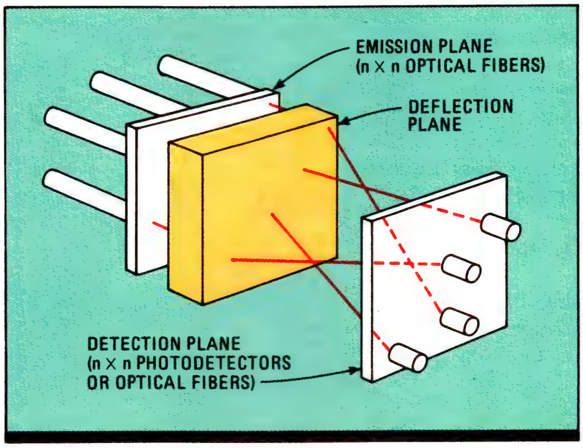
CORBEVILLE, FRANCE

A team of French engineers thinks it may be on the road to solving one of the most fundamental problems limiting the future of optical communications: how to switch large numbers of optical signals without reducing the bandwidth of the original signal.

The researchers, working at the Central Research Laboratory of Thomson-CSF in Corbeville, a suburb of Paris, have developed a scheme for optically deflecting the light beam carried by an optical fiber so the beam can be injected into any one of at least 1,000 other fibers. Thomson calls its system optical-beam steering using dynamic holography—it deflects light beams using a diffraction grating recorded by holographic means in a light-sensitive crystal.

The company's aim in developing the scheme is to find a way of relieving the bottleneck that occurs in switching optically transmitted communications. This could form the basis for an end-to-end optical switching system for potential use in a variety of telecommunications, data-processing, and data-communications areas.

The current method for switching optical signals involves converting them into electrical signals, switching them to new paths, and then using the switched electrical signals to drive semiconductor lasers that inject beams into fibers that carry them forward. The problem is that the communications bandwidth realized is limited to that of the electrical switching module and associated conversions, a figure inherently lower than what can be transmitted over an optical fiber. The only optical switches so far realized have been optomechanical, using mirrors. These are suitable for realizing only a handful of connections.



CROSSPOINT. Light beams from a matrix of input fibers are deflected by a bismuth silicon oxide crystal to selected fibers in the output matrix in Thomson's dynamic holographic switch.

Thomson's choice for the crystal is bismuth silicon oxide (BSO), because of three essential properties it offers. First, holographic images can be recorded and erased in a BSO crystal in real time. Second, the material is available in sufficiently large pieces to make it possible to switch a large number of points. Finally, it features inherent memory—connections once established are maintained even after the writing beams are turned off.

After a beam of light is emitted from one of the fibers upon entering the switch, it encounters a diffraction grating that is recorded in the crystal. By modifying the spatial frequency and the orientation of the induced grating, it is possible to change the direction in which the beam is diffracted along horizontal and vertical planes, thus causing its deflection toward the input of the desired fiber of the opposite matrix.

VISIBLE. The BSO crystal is not photosensitive at the near-infrared wavelength of semiconductor lasers used in telecommunications. The beams from two visible-light lasers write the grating that causes the deflection. These lasers use dye sources to provide an output with variable wavelengths from 535 to 575 nm. When the two beams interfere with each other in the BSO crystal, the grating they write there deflects the signal beam in a direction that is a function of their wavelengths. Thus, varying the wavelengths of the two writing lasers changes the deflection angle. Once the grating is written, the crystal becomes a passive optical switch.

The switching device is designed to connect two matrixes made up of n×n optical fibers, each ending in a microlens. The practical limit is somewhere between 1,000 and 10,000 fibers per matrix, according to Jean-Pierre Herriau, the engineer coordinating the project.

Thomson has developed a prototype that can switch a beam toward as many as 200 addresses with a switching time of about 20 ms—sufficient for standard telecommunications applications. Further research will center on optimizing the BSO material to raise diffraction efficiency, which is currently only 1%, to the 10% to 20% Thomson researchers deem necessary for communications applications. *–Robert T. Gallagher*

INDUSTRIAL CONTROL

SOFTWARE LETS IBM PC DO REAL-TIME CONTROL

HUDSON, N. H.

Universal Automation Inc. has come up with a software-development system with a flow-chart-based programming language that gives personal computers the speed necessary for real-time control. The development could give personal computers a fighting chance to replace programmable controllers in some industrial control applications.

The Hudson, N. H., company claims its system beats programmable controllers in both speed and flexibility. Programmable controllers, which have long ruled the roost for real-time control, use ladder-diagram programming to ease troubleshooting by technicians on the factory floor. But ladder-diagram programming, a language based on Boolean algebra, is time-consuming and very cumbersome for applications that involve data manipulation.

Makers of programmable controllers, such as Allen-Bradley Co., are struggling to increase functionality and ease of use. Some controller vendors offer software for setting up ladder diagrams on a personal computer, and then transferring them to the programmable controller. This cuts costs, but doesn't make it easier to manipulate data with ladder-diagram techniques.

"Ultimately, we're developing alternative control languages," says James Coburn, manager of processors and communications for Allen-Bradley's Programmable Controller Division, Highland Heights, Ohio. The eventual goal, he adds, would be to give end users the ability to create macros (which resemble subroutines) in multiple languages.

Universal Automation claims its programming language, called Flo Pro, will reduce setup times and provide more flexibility than ladder diagramming. In a typical task, Universal Automation's system allows a standard IBM Corp. Personal Computer to read 64 inputs, update 64 outputs, evaluate program logic, and restart the process in 10 ms. If the input/output numbers are raised to 512 each, the scan takes about 25 ms, the company says.

The key to Flo Pro's speed is the software, which keeps track of where it is on the flow charts at all times. This avoids the need to scan all logic for each step, as would a Boolean language, says Ron Lavallee, the company's president. So although personal computers have slower processors and I/O circuitry than programmable controllers, the scan rates meet or beat controller rates in most applications.

BUILT-IN DEBUGGING. The system is multitasking in that it allows a single task to be broken down into as many as 50 flow charts, which can execute simultaneously. Debugging features, such as the ability to freeze a program in midstream, are built in.

To use Flo Pro, users begin by describing the automation task in the form of a functional flow chart. The next step is to convert the flow chart into a executable flow chart consisting of numbered action and test blocks. The executable flow chart is keyed into the computer in response to a series of prompts from the language's interface.

Universal Automation admits its language will provide only small productivity gains in the automation concept stage. The major time savings comes in software development, however, where productivity gains from 25% to 75% are predicted. "The more complex [the task], the better we look," says Lavallee. "It also depends on how well people write flow charts."

What makes this process faster, says Lavallee, is that the user is merely concerned with what needs to be done rather than how to do it. "You don't need to know specialized programs," he says. "A mechanical engineer can pick it up and program it almost immediately."

The system will not immediately replace programmable controllers in harsh industrial environments, says Lavallee, partly because most personal computers are not rugged enough. But he believes clean high-tech industrial sites will provide a market. The systems are already in place at a hard-disk burnishing operation and an automated printed-circuit-board testing facility.

Along with the software package, Universal Automation is also making a number of interface modules and offers what it calls an automation controller, a unit that stands in for the computer for the execution of the program. The flow-chart programs can be keyed in on a separate personal computer and then downloaded to the automation controller. *–Craig D. Rose*

FLOWING. Universal Automation's Lavallee says flow-chart-based software doesn't have to scan logic for each step.

MILITARY

PENTAGON ISN'T GETTING MONEY'S WORTH IN R&D

WASHINGTON

Flying in the face of a 56% increase in Pentagon spending for research and development over the past four years is "a modest decline" in the U. S. standing in basic technology versus the Soviet Union. So says a report, released last week by the chairman of the House Armed Services Committee, that questions whether the nation has received an adequate return on its four-year, $1 trillion military investment.

Rep. Les Aspin (D., Wis.) released the 25-page compendium of statistics in conjunction with the start of a series of hearings designed to assess the Reagan Administration's unprecedented peacetime buildup. Aspin, critical of Pentagon procurement policies in the past (though he more recently spearheaded Democratic party efforts to toughen its stance on defense issues), has called hearings before the House committee's Defense Policy Panel in anticipation of shrinking Pentagon budgets.

Inside the overall 56% increase, measured in constant fiscal-year 1985 dollars, Pentagon funding of basic technology rose 63% in real terms between 1980 and 1985, Aspin estimates.

Yet Aspin's report concludes that there has been a technology decline based on the DOD's own comparisons of the relative Soviet-U. S. standing in 15 key military technology areas in 1980 and 1985. The DOD reports rate the U. S. as superior, equal, or inferior to the Soviet Union in these areas. In 1985, the U. S. position has deteriorated in three areas: microelectronic materials, electro-optical sensing, and submarine detection. Eleven other areas are unchanged, including laser technology (where the superpowers are believed to be equal), computers, telecommunications, optics, and signal processing. Only radar sensing improved. "By the Defense Department's own judgment, the results do not compare favorably with the investment made," Aspin concludes.

U. S. loses ground to Soviets despite hike in spending

The Pentagon quickly issued a response that does not specifically address Aspin's assertions concerning research and development spending, but does rebut his contention that "the one thing that clearly has grown in the weapons area is unit costs."

The DOD says that new equipment deliveries began during fiscal year 1984, and that "because, in general, this replaces older equipment, you would not expect inventories to rise." Citing the reduced cost of weapons such as the F/A-18 fighter and the AIM-9 air-to-air missile, the DOD argues that the cost of many weapons systems has decreased. "Progress has been made," the DOD rebuttal states. "Our military strength has improved over the past four years, but there is much more to do."

Peter L. Aseritis, who follows the military electronics market for E. F. Hutton & Co., New York, generally dismisses the Aspin report as politically motivated. Still, he agrees with its conclusions about a U. S. decline in basic technologies such as microelectronic materials. The Soviets have gained because they've had so far to go, he says, while the U. S. continues to push the state of the art.

Later this month, hearings will be held on how the present defense requirements can be reconciled with constrained resources. Next month, Aspin's panel will turn its attention to how the formulation of defense policy can be made "more a matter of rationality than improvisation." *–George Leopold*

COMPANIES

STRIKERS SLOW SPERRY DEFENSE WORK

NEW YORK

When the strike for higher wages and improved fringe benefits against Sperry Corp. by 3,300 employees—including 1,900 engineers—at two Long Island plants began on Sept. 12, both sides said it would be long, probably bitter, and possibly irreversibly damaging to both the company and the union. It is well on its way to fulfilling those gloomy predictions.

Into its fourth week without noticeable softening on either side, it is approaching the length of the six-week strike that hit Sperry in 1976. Bitterness is creeping into the public and private actions by both sides. Last Monday, Sperry imposed a news blackout. A police horse was slashed at one of the picket sites. At the company's request, a state supreme court judge issued guidelines to picketers instructing them to refrain from threatening or harassing nonstriking workers at the two affected plants in Lake Success and at Long Island's MacArthur Airport in Bohemia. The company has issued a statement that it might move its work on military contracts off Long Island to other, nonunionized plants. Sperry depends on defense contracts for 95% of its work at the plants.

MOVES UP. Joseph J. Kroger's appointment as president and chief executive officer of Sperry was part of a corporate reorganization.

Observers expect the pressure from both sides to create lasting ill will: "It will leave a legacy of bitterness," says Michael Geran, an analyst for E. F. Hutton.

For its part, Sperry has to balance the increasing competition and a shrinking market for defense contracts with the fact that the Long Island workers (the only unionized segment of a company that employs 60,000 people) are demanding more than the company thinks it can handle.

"With the change in technology and systems development, the rate of spending in the defense industry is scheduled to slow down," says Geran. "Over a period of time, a greater proportion of contracts will be information-system-based. This also will lead to differences of opinions between management and labor in terms of how to manage the transition."

Also inexorably tied to the strike are the general fortunes of Sperry. The company calls itself the world's fourth largest computer company, with computer-related revenues of $4.2 billion, yet observers consider it a weak member of industry because, for one thing, it is tied to rapidly aging technology.

NO MERGER. Still, Sperry is reputed to employ some of the industry's best engineers, making it a takeover target. Last June, a merger attempt with Burroughs Corp. failed. Such a move would have created the world's second largest computer maker behind IBM.

One result of the failure was the naming of Joseph J. Kroger as president and chief executive officer. Kroger, formerly president of Sperry's Information Systems Group, served as the company spokesman during the tense days of the Burroughs merger collapse. Some observers see his appointment as part of a plan to make Sperry more attractive to a possible buyer.

But what kind of blow will a long strike deal? Already, it is taking its toll, and Sperry admits that its reliance on senior engineers to do all the work has created a difficult situation. Sperry is falling behind schedule, which led to the company's statement about moving part of its operations away from Long Island.

'The strike will leave a legacy of bitterness'

"From the very beginning, our single focus has been to meet our contract commitment with the Department of Defense," says Nancy Macenko, Sperry's manager of communications. "Of course, we cannot fulfill our commitments without the other half of our work force, namely the engineers. In effect, what we said is that if the strike does not end within a reasonable period of time, we will consider moving our contracts to other locations where they can be fulfilled."

The union has countered that the company threat is mere bluster and that it lacks the engineers and facilities to transfer the government work to other locations. In fact, says Henry Zylla, president of Local 444 of the International Union of Electrical, Radio, and Machine Workers, if the strike is allowed to continue, Sperry will suffer the loss of a significant number of engineers. "We have been told that a lot of our people are leaving. We will lose hundreds. In 1976, we lost 350 engineers and that was with a smaller base." Zylla contends that each engineer lost will cost the company $12,000 to replace.

However, "We don't have any firm evidence that any engineers have left," Macenko counters. "At this point, that is merely picket-line speculation."

But the true cost will be in terms of morale, according to Zylla. "Even when they go back to work, these people will still be unhappy."

–Jesse J. Leaf and Gina G. John

TESTING

TERADYNE TUNES SYSTEM FOR MEGABIT MEMORIES

LOS ANGELES

Many manufacturers of dynamic random-access memories, as they push toward the volume production of 1-Mb parts, have come upon a very sticky problem in the probe-test cycle for the big devices. They say it is very difficult to analyze the failure data of the redundantly configured memory arrays and repair them during the same cycle with an attached laser system. Available test systems are too slow to do the job.

Teradyne Inc. will unveil a package this week for its J386 memory test system that targets this and other problems of testing megabit parts. A number of Japanese tester vendors have, like Boston-based Teradyne, added parallel-testing capabilities to offset the longer testing times for megabit RAMs. But Teradyne has also done extensive software work to shorten the test-cycle time for each chip.

The Teradyne enhancement is timely, because the first appearances of the 1-Mb chips [*Electronics*, Sept. 30, 1985, p. 30] are just now bringing testing problems to the fore. The Dual Megabit Catch RAM hardware-and-software package adds $40,000 to the $200,000 price of a J386 memory tester, more than 300 of which have been sold. The term Catch RAM refers to the capture of errors during the real-time bit-mapping process.

Earlier versions of the Teradyne tester did not work fast or accurately enough even for simpler 256-K chips, and could not handle parallel testing necessary to boost throughput to acceptable levels. Engineers at Teradyne's Semiconductor Test Division started addressing these shortcomings more than a year ago and consider the project as challenging as any yet tackled.

The most difficult part of the task was software development, particularly writing a fast redundancy algorithm that in a few hundred milliseconds can determine all possible solutions for repairing a device. Overall cycle time per chip for the enhanced tester is about 350 ms, not including laser repair, compared with a full second for previous versions. Most individual test functions within the program take about 60 ns.

HARDER THAN IT LOOKS. Boosting tester performance for 1-Mb DRAMs is a task "everyone thinks is easy, but is tough," observes Jerry Hutcheson of VLSI Research Inc., San Jose, Calif., a consultant who closely follows semiconductor testing. The Japanese, however, have not been deterred.

Advantest Co. of Tokyo, which before Oct. 1 was called Takeda Riken, last December began shipping its T3332 test system, which can handle 1-Mb RAMs. Advantest claims that close to 150 systems have been delivered—at an average cost of about $500,000—but admits that many (other sources say most) of those are set up to test 256-K chips.

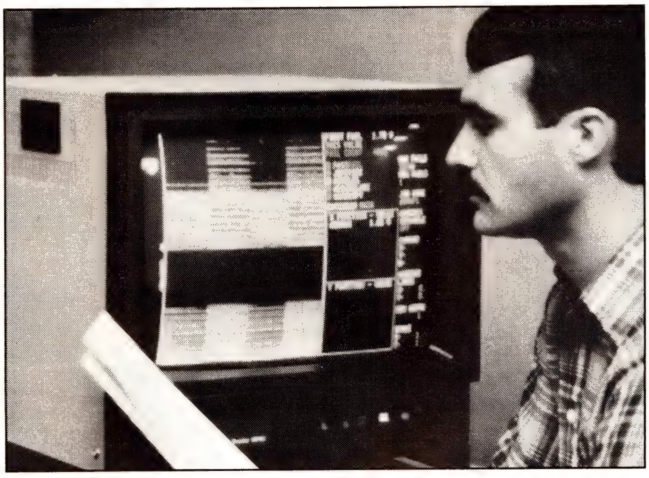
Michiaki Chamoto, manager of advanced test equipment sales for Advantest, says that the major design change for this system was provision for two test heads and two eight-sited autohandlers, so 16 chips can be tested at once to lower per-device testing costs.

Ando Electric Co., also of Tokyo, has been marketing its DIC-8042 since April for roughly $458,000 per unit. Also accommodating up to 16 1-Mb devices at a time, this system also features on- or off-line redundant memory testing.

Two other Japanese companies who have brought such testers to market are Hitachi Electronics Engineering Co. and Minato Electronics Co. Hitachi's system, offered beginning in June with the same general features as the Advantest system, is expected to be used mostly in house. Minato says it began marketing its 94000 system last year.

Teradyne has not taken parallel testing as far as Advantest and Ando. The structure of the Catch RAM allows the system to accommodate only two 1-Mb chips or four 256-K devices at a time.

A feature of the tester that should be useful in device characterization, says product manager Robert Powers, is the display, "where you can actually see what's going on in the



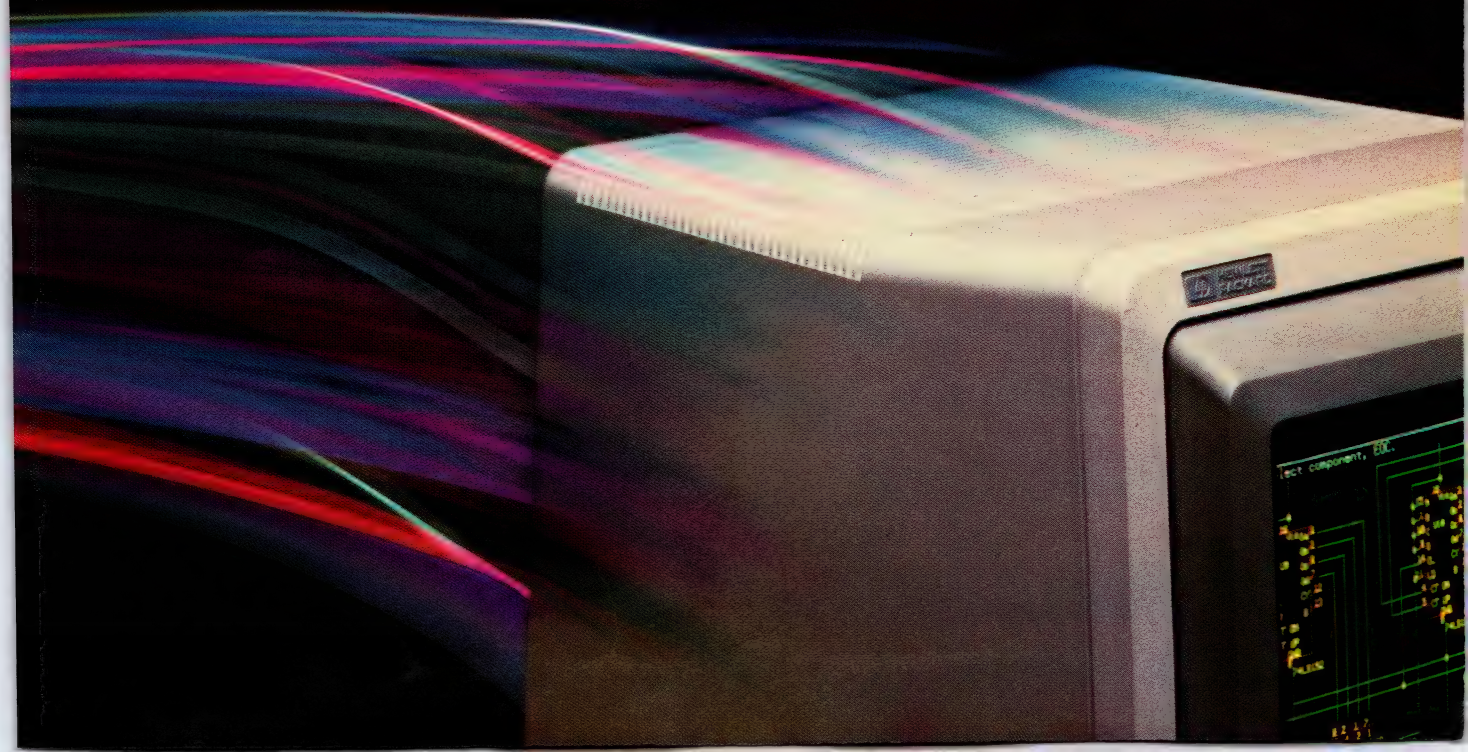
MAPPING BITS. Real-time bit mapping can be observed graphically when Catch RAM is added to Teradyne's J386 memory test system.

Name the computer that's so modular and expandable it lets you upgrade from 16-bit to 32-bit processing...

Expand from .5 to 7 Mbytes of memory...

Or go from monochrome display to high-resolution color graphics...

All in a snap...



Introducing the HP 9000 Series 300

The computer that

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chip." A 16-to-1 display compression of memory cells shows on a color monitor the real-time bit mapping in progress.

At present, the tester is designed to handle only 256-K-by-4-bit parts, the configuration potential customers most requested. None asked for a by-1-bit test configuration, though many have these chips in the offing. Teradyne officials say there is no reason why they cannot supply this test configuration as well.

While Teradyne will not yet discuss further megabit tester improvements, especially those that will handle more parts in parallel, it is a certainty that these will be forthcoming, say observers. "We are making a big effort," says Powers. "We haven't written off the memory business."

–Larry Waller and Michael Berger

PACKAGING

CAN SURFACE MOUNTING SAVE EUROPEAN MAKERS?

EINDHOVEN, THE NETHERLANDS

Europe's electronics-equipment producers have watched their market shares slide over the past half-dozen years as Far Eastern companies, in particular, have undersold them. But Philips, Europe's top producer of both components and electronic equipment, says there is a way to counter the decline: slash production costs through a massive switch to surface-mounted-device technology. And to show the way, the Dutch company's Electronic Components and Materials Division (Elcoma) intends to intensify its already-strong commitment to SMD.

Elcoma, based in Eindhoven, will bankroll the effort by spending between $200 million and $300 million on the technology over the next five years. Already, all of Elcoma's production facilities around the world are making at least some surface-mounted devices. But one of the first moves is the construction of a $25 million factory in Roermond, Holland, devoted to SMD multilayer capacitors. Over the next two years, several other Philips plants around the world will be converted to produce nothing but SMDs. By 1987, every Philips component that can conceivably be packaged as an SMD will be.

Along with producing SMDs, Philips' crusade includes building the pick-and-place machines necessary for SMD production lines as well as a heavy promotion effort to sell the advantages of SMD to equipment makers.

PARTS BY THE BILLIONS. Of course, the technology that Philips sees as Europe's salvation translates into a hefty market. According to the company's estimates, the worldwide demand for components that could come in SMD packages will reach 215 billion pieces this year. By 1990, the total is expected to climb to around 290 billion units.

Actual SMD sales, however, are more like 45 billion units worldwide this year. They figure to rise to 115 billion by 1990, Philips says, an annual growth of 20%. By the end of this decade, SMDs should take about 40% of the total components market.

MISSIONARY. Philips's Henk Bodt sees surface-mounted devices as the salvation for Europe's electronic-equipment makers.

Japan is already ahead of the rest of the world in the use of the new devices. The current SMD penetration there, Philips says, is 30% and should be around 50% by 1990. In the U. S., the respective figures are 15% and 30% of an extremely large components market. And in Europe, the rise in SMD penetration is figured to go from 14% this year to 35% in 1990.

Besides manufacturing SMD components, Elcoma is continuing its effort to sell equipment makers on the benefits of SMDs, whose compact packages drastically reduce printed-circuit-board size and can cut assembly costs by as much as one half. Philips began to proselytize in 1983 with a series of conferences and seminars that covered more than 80% of Elcoma's main customer base outside Japan. Several thousand people, representing 1,000 companies, attended the events.

Elcoma will step up its educational mission along with its manufacturing mission. A two-year program of weekly courses at several Philips centers in Europe will begin this month. Philips expects between 6,000 and 8,000 engineers to attend. There will also be workshops offering practical information and hands-on experience in circuit design and production using SMDs.

Finally, Elcoma has been stressing the development of placement machines. The company's first, and fastest, unit can place 500,000 devices an hour, easily meeting the needs of big companies for at least the next three to four years. In the coming months, Elcoma will add modular and highly flexible machines to its equipment lineup to suit smaller manufacturers.

NOT JUST FOR MONEY. Although Philips is in business to make money, Henk Bodt, senior managing director of Elcoma, maintains that SMD is not just a new business opportunity or market segment. He regards the technology as a weapon to help stave off the attacks by Japanese manufacturers and other Far Eastern companies against the Western electronics industry.

If Europe and America fail to embrace manufacturing technologies that can "reform and salvage our home-based production by making it cost-efficient and competitive again, then no amount of protectionism will save the Western industries from the Japanese invasion," Bodt says.

A few figures point up Bodt's concern. From 1978 to 1984, the world's electronic-equipment production rose from about $100 billion to $240 billion. Europe's share during this period fell from 33% to 23% of the world market. It lost 7% of the consumer-electronics industry to the Far East, while 3% of the electronic-data-processing sector slipped away to the U. S.

Cut in parts cost would stave off Far Eastern firms

But the U. S., too, has had problems, particularly in consumer electronics, Bodt says. American producers once regarded it as a low-technology sector. They also felt low labor costs were Japan's major advantage. So they moved production offshore to low-labor areas to remain competitive.

This, however, could not save U. S. consumer electronics. Many companies missed the trend to high technology in consumer products and failed to make the investments necessary to keep pace. In the mid-1960s, Bodt points out, shoppers had a choice of TV sets from a score of U. S. manufacturers. Today, he says, imports dominate and the U. S. brand names on dealers' shelves can be counted on the fingers of one hand.

–John Gosch

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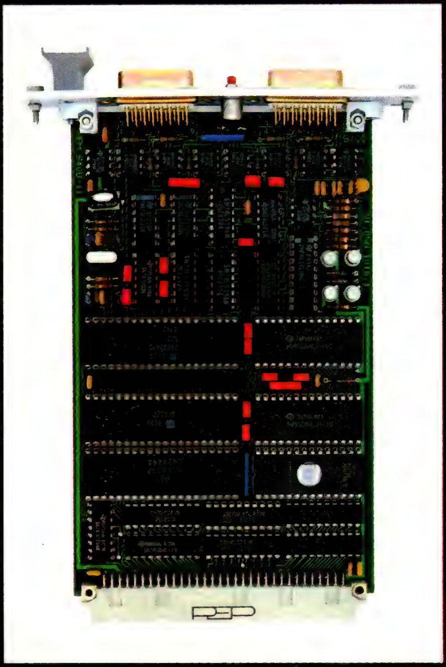

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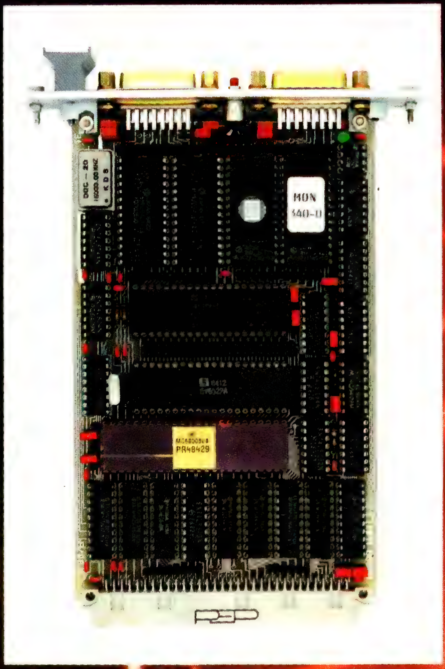

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- MC68008 CPU (8...16 MHz)
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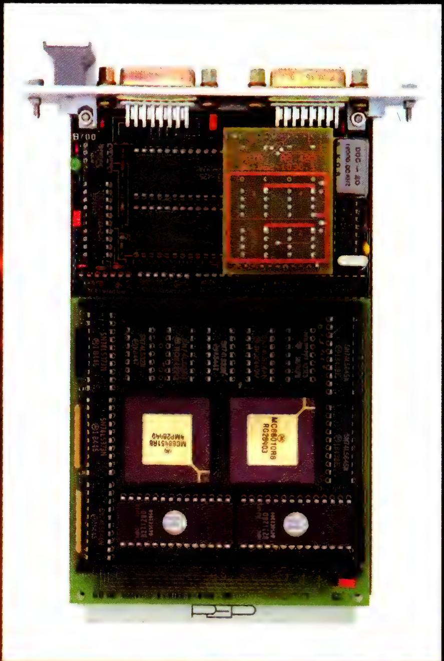

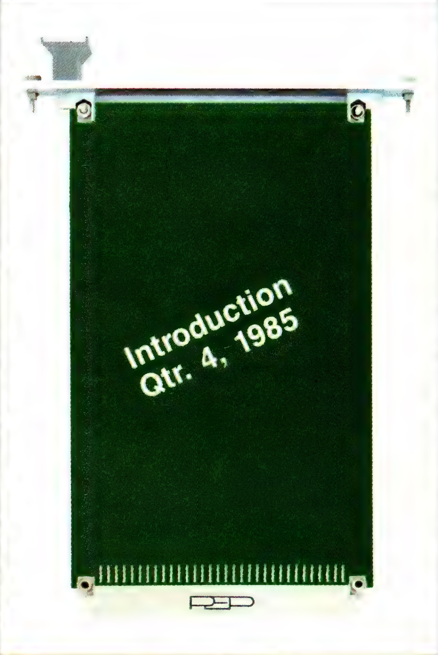

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- Bus arbitration logic for multiprocessor applications
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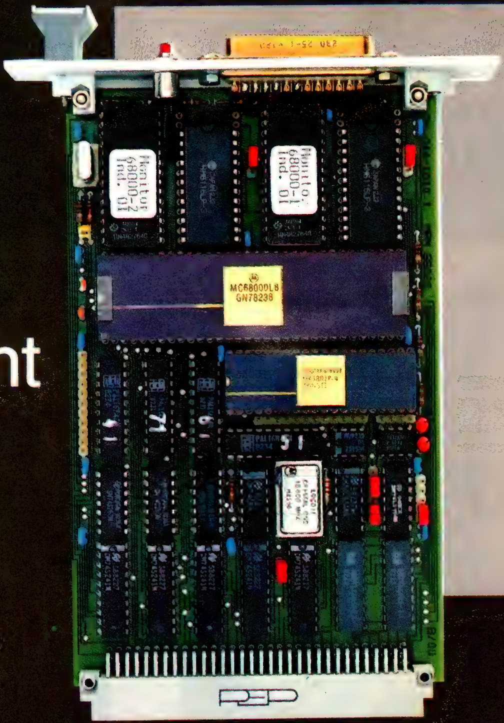

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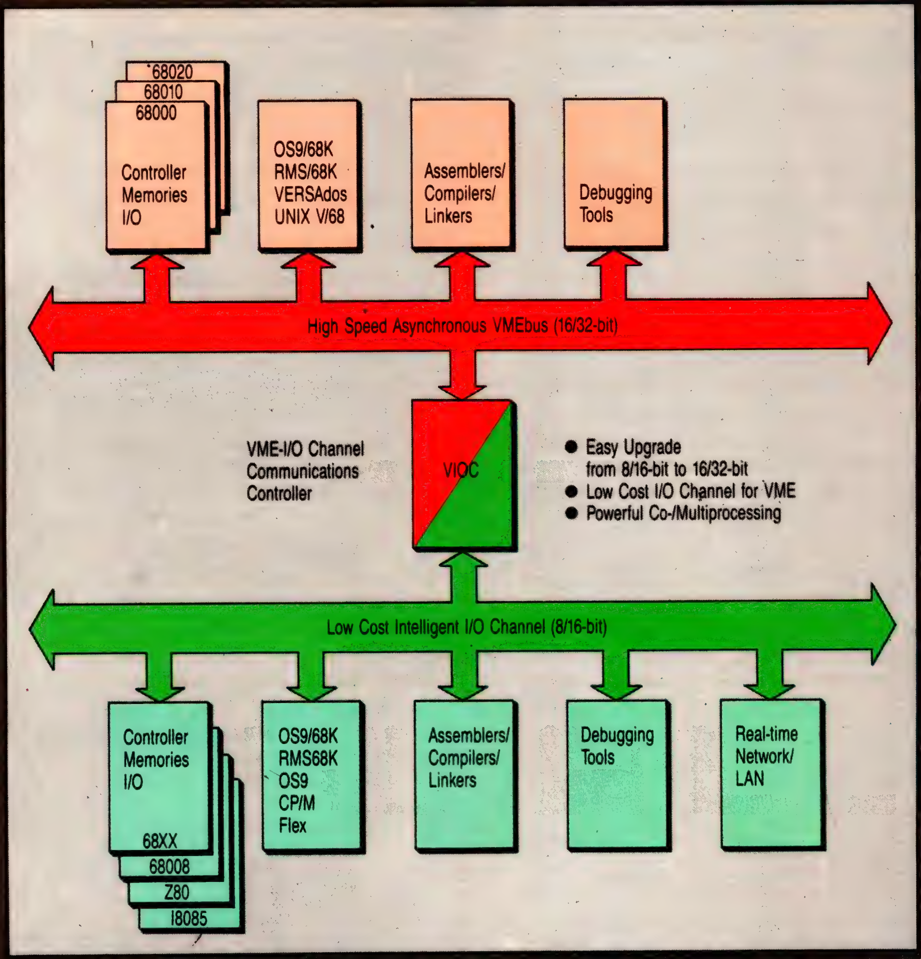
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ELECTRONICS WEEK

BLUE CHRISTMAS AT NATIONAL

Following a net operating loss of $47.6 million in its just-ended first fiscal quarter, National Semiconductor Corp., Santa Clara, Calif., announced seven additional days of plant closings for the Christmas and New Year's season. That will make 39 days of plant closings this calendar year. The company, which posted additional losses because of interest and tax payments, had a total loss of $53.5 million for the quarter, or 59¢ per share.

EMULEX ALLEGES DEC VIOLATIONS

Claiming that Digital Equipment Corp. has violated federal antitrust laws, Emulex Corp. has filed several counterclaims to DEC's patent-infringement suit [*Electronics,* Sept. 9, 1985, p. 21]. Emulex, Costa Mesa, Calif., makes controllers and mass-storage and communication products for DEC computers.

In its filing, Emulex says that the Maynard, Mass., company already dominates 75% of the peripherals market that Emulex and other suppliers address. It also claims that the computer maker engaged in predatory practices—including illegal equipment tie-ins, bad faith misuse of patents, and abuse of the legal process by trying to enforce invalid patents.

RENAULT TO BUILD SOVIET ROBOTS

Régie Renault, France's principal automaker, will likely win a contract in the weeks to come to retool the Moskvitch car production plant near Moscow. Renault executives hope the contract, totaling some $50 million worth of welding equipment and robots, will lead to a more extensive deal whereby the company would sell the USSR an automobile motor production facility for a figure more than double the present contract. The deal is part of a continuing effort by the French government to use technology sales to reduce its trade deficit with the USSR, which rose to a record $500 million last year [*Electronics,* July 15, 1985, p. 38].

RCA RESTRUCTURES SOME BUSINESSES

RCA Corp. has restructured some of its electronics and communications business and phased out some product lines, citing competitive pressures and continued losses in its Broadcast Systems Division. RCA will also close its West Palm Beach, Fla., plant next year. It also merged RCA Cylix and RCA Globcom to consolidate facilities and streamline its operations.

NTT BUYS SECOND CRAY MACHINE

Nippon Telegraph & Telephone Corp. will spend an estimated $8 million for its second Cray Research Inc. supercomputer. Last year, NTT bought a Cray X-MP 22 for use in its research and development laboratories. Now the Japanese communications giant plans to buy an X-MP 1 from the Minneapolis company's Japanese subsidiary, Cray Research Japan Ltd., for the same purpose. NTT bought just $133 million worth of U. S.-made equipment last year and is not expected to match that total in 1985, hence is looking for ways to boost the figure.

MOLEX SIGNS WITH INDIAN COMPANY

Claiming to be the first major international connector manufacturer to join with an Indian company, Molex International Inc., Lisle, Ill., has signed a joint venture agreement with Jay Electric Wire Corp. of Bombay. The joint company, to be known as Jalex Connector Systems Ltd., will set up a plant in the state of Karnataka in the second half of next year. Jalex, which will eventually have 200 employees, will manufacture and market a line of standard connector parts and assemblies.

JOINT VENTURE SET IN AI SOFTWARE

Mad Intelligent Systems, San Jose, Calif., will adapt its 80286-based work stations for artificial-intelligence tasks through a joint venture with Advanced Information & Decision Systems, a Mountain View, Calif., AI consulting firm. The two have formed Ariel Technology to develop AI software. Mad has also named Sandra Cook, an AI specialist from SRI International, to the new position of vice president for expert systems. Cook will develop AI-based systems for the financial community.

MOTOROLA QUITS SOUTH AFRICA

Motorola Inc. has joined the list of U. S. companies pulling out of the Republic of South Africa. Bowing to pressure from stockholders, the Schaumburg, Ill., company last week said it is selling Motorola South Africa, its wholly owned subsidiary there, which manufactures mobile and portable radios in a 44,000-ft^2 plant with 225 employees. The buyer is Allied Technologies Ltd., a South African electronics and telecommunications company, which will continue production under a manufacturing license. Motorola will continue to export to South Africa.

SILICONIX BUCKS RECESSION

While other semiconductor companies are announcing devastating losses this year, Siliconix Inc. reports record sales in its third fiscal quarter of $26.3 million, up 11% from a year ago. The Santa Clara, Calif., manufacturer of FETs, gate arrays, smart power integrated circuits, and MOS power transistors reaped sales of $77.8 million in the first nine months of this year, up 20% compared with a year ago. Because of a one-time tax credit last year, net income was down slightly this year at $2.3 million for the third quarter compared with $2.5 million for the same period last year.

DSC CUTS INCOME, STOCKHOLDERS SUE

DSC Communications Corp. is trying to keep a dispute with a major customer from erupting into a lawsuit, but the Richardson, Texas-based telephone switch maker may still wind up in court. Two DSC shareholders have filed federal suit in Dallas, alleging false and misleading financial statements were issued by the firm in 1984 and 1985. Early this month, DSC announced that a dispute with a major telecom customer—reportedly GTE Sprint—was causing it to reduce stated revenues and earnings for the first half of 1985 and the 1984 fiscal year. Earnings were restated downward by $28 million for the first half of 1985 and $13.5 million.

SEMI TO FORM EUROPEAN CHAPTER

Semiconductor Equipment and Material Institute Inc., based in Mountain View, Calif., has set up a European Steering Committee to guide the formation of a European chapter. The committee, which is being chaired by Fritz Vieweg-Gutberlet of West Germany's Wacker Chemtronic AG, consists of European suppliers of semiconductor-processing equipment and materials. Other companies represented in the committee are ET Electrotech, UK; Dynamit Nobel Silicon, Italy; Alphasem Group, Switzerland; BSE, Belgium; L'Air Liquide, France; and ASM, the Netherlands.

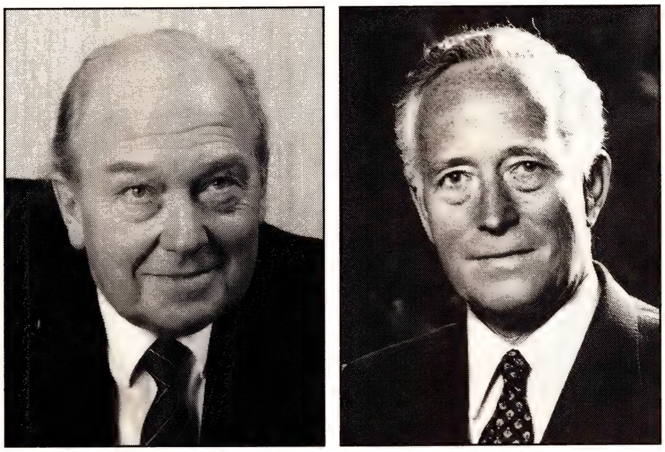
HOW STC AIMS TO GET OUT OF ITS CASH-FLOW CRISIS

TROUBLED BRITISH ELECTRONICS CONGLOMERATE LOOKS TO NEW CEO WALSH TO LEAD TURNAROUND

LONDON

Hit hard by the current slump in the electronics industry, Britain's STC plc has been looking for a new chief executive since Sir Kenneth Corfield resigned in August in the wake of a boardroom revolt over the company's poor performance. The search is now over: Arthur Walsh, formerly chief executive of GEC Electronics Ltd., a subsidiary of General Electric Co. plc, is taking on the job of turning around the troubled electronics company.

Walsh has spent his professional life at GEC, and is little known outside the company. Yet the 59-year-old Walsh could have exactly the qualities STC needs if it is to survive, believes one senior GEC executive. The former associate, who declined to be identified, says Walsh is a combative character who enjoys a challenge and gets things done. From the moment he walked into STC's swank London headquarters in the Strand at the start of this month, Walsh has been busy.



NEW MAN. Following the resignation of Sir Kenneth Corfield (left) as chief executive, STC has chosen former GEC Electronics Ltd. chief executive Arthur Walsh to turn around its troubled operations.

Whereas Corfield played the strategist, Walsh is more pragmatic. In addition, he comes from a company where financial controls are stringently applied. And, observes his ex-colleague, he will not repeat one Corfield mistake. "When you pursue a grand strategy, the one thing you must not do is surround yourself with 'yes-men.' Walsh likes people who argue their corner, and he tends to back them. But if they do not deliver, he will not accept their excuses."

Walsh will have his hands full. "STC is at a crossroads," says Alec Park, STC's executive director in charge of financial controls. "It can go forward and exploit its technology base or go back. But given the relentless change in the electronics industry, it cannot stand still." It will be Walsh's task to decide on STC's direction and drive the company toward its chosen goal.

STC is in the middle of a cash-flow crisis. Its problems have been precipitated by two factors. First, a general industry recession hit all its divisions, particularly its telecommunications and components operations. Pretax profits at the midyear mark dropped sharply to $30 million, down from $108 million for the same period last year.

Second, an ambitious acquisition and expansion program that netted Britain's International Computers Ltd. plc has drained cash resources. Funds have also been absorbed in capital projects, such as an $85 million chip plant in Footscray. STC's cash outflow in the 1985 first half totaled $263 million, using up a $239 million cash infusion from a stock issue earlier this year and forcing it to increase borrowings by $24 million to $393 million.

STC has also had to make provisions in its balance sheet for the cost of disposing of its money-losing operations. Closing operations and divesting other businesses caused an extraordinary loss of $42 million in the first half, which wiped out operating profits of $30 million and resulted in a $12 million net loss (see chart).

STC chairman Lord Keith of Castleacre, who had been acting chief executive since Corfield left the company, made a start at getting the $2.84 billion company back on the rails. Plans were announced to trim corporate overhead by $100 million a year and to sell off as much as 15% of its operations.

Accountants Peat, Marwick, Mitchell & Co. have been called in to help identify the core businesses on which STC's management should focus. And consultants from Arthur D. Little Inc.'s London office will review STC's component business, in particular the semiconductor plant being built in Footscray. "We have to move away from long-term strategies and look more carefully at our medium-term opportunities and needs," says Lord Keith.

The wheel of fortune has turned all too quickly for the former ITT Corp. subsidiary. STC became an independent British company in 1982, when the U. S. conglomerate sold most of its holdings in Britain.

BROADER BASE. Corfield embarked promptly on an acquisition program aimed at transforming STC from a stodgy manufacturer of telecommunications gear into a broadly based information-technology group. The convergence of telecommunications and data processing would create major business opportunities for a company with fingers in both pies, Corfield believed.

Corfield's boldest move came last September, when he purchased ICL, Britain's flagship computer group [*ElectronicsWeek,* Aug. 20, 1984, p. 59]. ICL has had a crisis-strewn history, so STC's move was greeted coolly by industry analysts. Yet under the hard-driving leadership of Robb Wilmot, ICL's managing director, it has recovered well from an anemic market position. Moreover, Wilmot was pushing ICL into data networking, which is where STC was moving. "I have never seen such a perfect fit," said Corfield at the time of the takeover.

Ironically, STC quickly ran into trouble after its purchase of ICL. But its problems were with its own businesses, not its acquisition. STC's telecommunications division in the past year has reported the worst performance of any STC division, with profits dropping to $10 million from $37 million. Its telecommunications switching business is based on the TXE-4, an analog exchange nearing the end of its life: British Telecom plc is switching over to the System X digital switch made by Plessey Co. plc and by Walsh's former employer, GEC.

William Dixon, an analyst at Scott Goff Layton, in London, believes the TXE-4's business should have been milked as a cash cow. Instead, STC is extending its product life with an upgrade. The startup costs of this upgrade program have been heavy, but STC recently sold another $71 million worth of TXE-4 systems.

Sales of other telecommunications products, such as Telexes and telephones, were down 30% in this year's first half. In Dixon's view, these businesses should be sold. "STC must sell enough of their businesses to leave a clean balance sheet. If they do not, they could staunch losses for a while, but the company would end up by going bust."

STC's components and distribution also should be put on the block to raise cash, says Dixon. These businesses are basically salable and sound, but the recession has reduced their total profits from $11.1 million to $4.6 million in the first half of 1985. Still, the company's laser-diode business supports products at STC's systems companies and is unlikely to be included in any divestiture. But STC may no longer be able to afford the luxury of its own microcircuit business. "It is obviously something we will look at," says Lord Keith.

The soundest of STC's traditional businesses may well be its submarine cables and fiber-optic transmission activities, which are part of the international communications and services division. Though sales for the first half of 1985 fell to $16 million from $22 million, the division has fundamental strengths. Fiber-optic transmission was pioneered at STC's Harlow Laboratory, and the company has remained at the fore in this technology.

Compared with STC's traditional businesses, ICL is a good income generator, contributing over half the parent's profits. "It is the brightest star in the STC sky," says Andrew Learoyd, an analyst with Panmure Gordon & Co., a London brokerage. Moreover, ICL's One-Per-Desk executive work station and Series 39 mainframes, both Wilmot-inspired products, have been well received and look like good revenue producers.

TOP PERFORMERS. The One-Per-Desk work station, for example, has so far racked up $42 million in orders, while the first year's production of the Series 39 was quickly sold. In the year ahead, the Series 39 will make an increasing contribution to profits, says ICL's new managing director, Peter Bonfield. He succeeded Wilmot, who is now a part-time chairman of ICL.

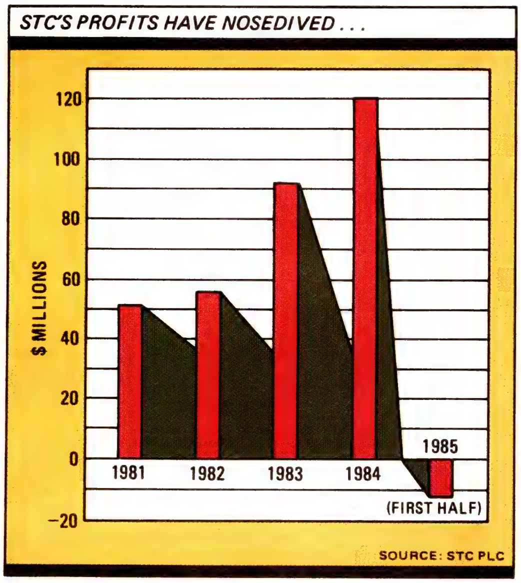
Corfield's ambition, however, was not just to add another business. It was to achieve synergistic growth by melding the two organizations. To make a coherent business strategy of this concept, he formed a planning group composed of executives from both STC and ICL.

So far, the group's one major achievement has been to set up STC Network Systems, a $70 million operation drawn from six units within the two companies. The new unit combines skills in network management, software design, private-branch-exchange networking, local- and wide-area-networking technology and value-added networks.

Network Systems will supply VANs, electronic fund-transfer systems, integrated data-communications networks, and the like. The division will address a market estimated to be worth $80 billion by 1990, STC says, $20 billion of which will be based in Europe. "We have spent the last six months defining our strategy, and we are now putting all the elements of that strategy into place," says Nigel Horne, STC's director of corporate development.

But success will not be easy as the new group will be taking on the likes of Philips, IBM, and British Telecom. STC and ICL are also collaborating in the design of second-generation executive work stations, an area in which both companies have products. Other product developments will take time to come through. *–Kevin Smith*

STC'S PROFITS HAVE NOSEDIVED . . .



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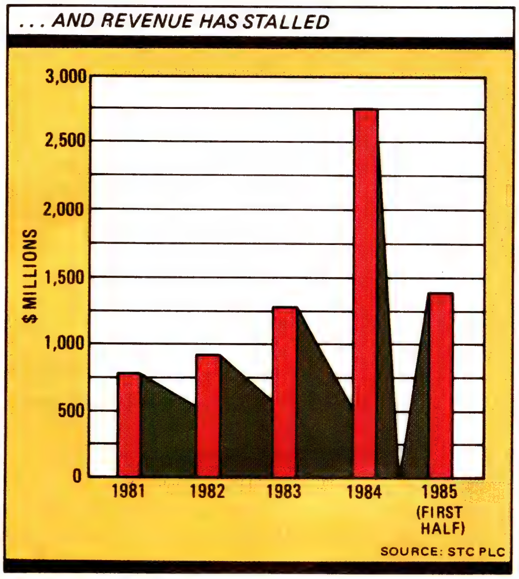

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BOTTOM LINES

JOB-SEARCH SERVICE TO SPAN THE PACIFIC

U. S. electronics companies may soon be able to tap into a new source of workers: entrepreneurial engineers and technology managers in Japan who want jobs in the U. S. International Business Information Service. IBIS, a Palo Alto consulting company, has developed a job-search service (in conjunction with Hamlin Associates, a Palo Alto executive search firm) that will work in Japan and the U. S., matching American companies with Japanese workers. "In Japan, there's a very firm belief that true innovation comes from the U. S.," says Mikiko Sato, president of IBIS. "A lot of Japanese technology professionals want to come to the U. S. for that reason."

UNGERMANN-BASS BUYS 20% OF ALLIED

Ungermann-Bass Inc., the Santa Clara, Calif., supplier of general-purpose local-area-network products, has purchased 20% of Allied Data Communications Group Inc., Norcross, Ga., from its founders for an undisclosed amount of Ungermann-Bass common stock. Ungermann-Bass said it also received options to buy another 10% of the Georgia company. Allied designs and installs cable plants for LANs, including the Ungermann-Bass Net/One communications system. More than one third of Allied's revenue comes from subcontracting work it performs for Ungermann-Bass.

FRENCH COMPANY INVESTS IN TELMOS

Telmos Inc., a Sunnyvale, Calif., maker of high-voltage chips and analog-to-digital semicustom arrays, has completed a $6.1 million financing. Of this, $4.1 million came from Merlin Gerin, a Grenoble, France, manufacturer of uninterruptible power supplies. Telmos plans to use the funds to boost its working capital and for building expansion. Telmos said the two companies are discussing a joint-venture design center in France to design products using a 200-V CMOS ADC array product line from Telmos.

APPLITEK RAISES ADDITIONAL FUNDING

Applitek Corp., a producer of local-area-network systems, raised $3.3 million in additional financing. The Wakefield, Mass., company said this brings to over $15 million the amount it has raised from investors. The new funds will be used to increase its manufacturing capabilities, it said.

PLAYERS

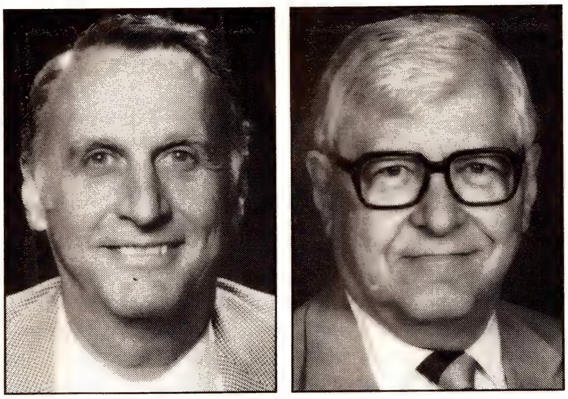
SPEAKING OUT IS KEY PART OF SWIFT'S JOB

SCHAUMBURG, ILL.

The U.S. electronics industry must guard against work-force obsolescence if it is to remain competitive in rough-and-tumble worldwide markets. So goes one of Robert N. Swift's favorite themes. Swift, who is Motorola Inc.'s new 61-year-old chief corporate staff officer, is responsible for all corporate staff functions except personnel, finance, and law.

As the successor to John R. Welty, who retired early this month, Swift says he views speaking out on industry issues as part of his new job. And as a Motorola executive vice president and director of personnel since 1977, it's not surprising that he has some things to say about the people side of the world competition formula.

"I've got strong feelings about the potential for obsolescence of the American work force," he says. "In the electronics industry, we're in such a dynamic environment that our knowledge becomes obsolete much sooner than it does in the smokestack industries, for example. One of our challenges is to make people understand that the education has just begun when they leave college."


MOTOROLA TRANSITION. Robert N. Swift, left, succeeds John R. Welty as chief corporate staff officer of Motorola Inc.

Swift has several reasons for concern, among them "an absolute dedication to education" in the Japanese culture and the fact that Japanese schools produce three to four times as many engineers as the U.S. "We've got to sharpen up," he says. Among the solutions, he sees electronics-industry support for universities and high schools as well as strong internal corporate training and education programs.

When it comes to speaking out on industry issues, Swift has some big shoes to fill. Welty, who now plans to teach and consult from a new home in Scottsdale, Ariz., was known in the job as a strong and frequent critic of the Japanese and a spokesman for the U.S. semiconductor industry. Among other positions, Welty was one of the founders and first chairman of the Semiconductor Industry Association in 1977 and was general manager of Motorola's Semiconductor Products Sector from 1975 to 1981.

Besides his emphasis on the work force, Swift brings to the job an international perspective and a background on the communications side of Motorola's business. A 23-year veteran of the company, he was director of international operations for three years, beginning in 1970. That was preceded by sales and administrative positions within the company's Communications Sector, which Swift joined in 1952 as a sales engineer. A native of Chicago, Swift earned a bachelor's degree in marketing from Northwestern University in 1948.

With responsibility for a broad range of areas, including strategy, marketing, research and development, patents, government relations, public relations and advertising, computer systems, manufacturing, and facilities, Swift likens his new job to "remodeling the bicycle while pedaling it."

"I'll probably be a lot smarter in three to six months," he says of his new duties. But there's one thing he already knows for certain: "It doesn't do you much good to have a fine business strategy if you don't have the right people to make it happen." *–Wesley R. Iversen*

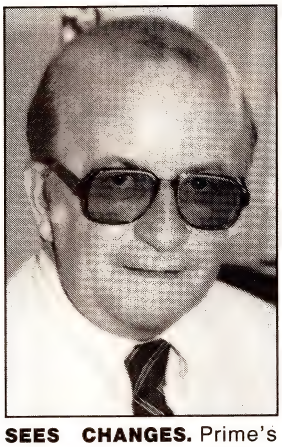
KNOWLES BOOSTS CAD/CAM AT PRIME

NATICK, MASS.

Ask Andrew Knowles, vice president of computer-aided design and manufacturing at Prime Computer Inc. about his market sector and he'll likely hand over a paper he wrote in 1971 titled "The Minicomputer and the Engineer." The historical perspective is relevant, he points out, because CAD/CAM evolved from a minicomputer application to a separate market.

A look at Prime illustrates the trend. Not widely known as a CAD/CAM supplier, the company nevertheless expects to do between $140 million and $150 million in this market this year, up from $105 million last year, which in turn was a 35% increase over the previous year. Knowles has headed the Prime effort since February, when his group's charter was expanded to include work stations and terminals.

Prime's healthy growth is coming at the expense of the pioneering CAD/CAM companies that developed turnkey systems and grew rapidly along with the market. "People who bought from turnkey vendors now say they want to do more with their systems," Knowles says. That includes office automation, data management, and communication capabilities, all of which are offered by the full-service computing companies such as Prime.


SEES CHANGES. Prime's Knowles has a plan for competing against IBM.

Knowles, 49, earned his EE degree from the University of Massachusetts and went to work at RCA Corp. He moved on to Digital Equipment Corp., where he worked for 15 years, most recently as product line manager for the PDP-11 and as vice president and group manager of the small systems group. Before joining Prime in October 1984, Knowles was briefly president and chief executive officer of Lexidata Corp., the Billerica, Mass., graphics-terminal manufacturer.

From his long experience as an applications engineer and as a marketer, Knowles sees CAD/CAM as an evolution toward a greater dispersion of functions and eventually leading to computer-integrated manufacturing, which will do everything from produce parts to handle payrolls.

Among the biggest challenges facing any company in the CAD/CAM business is how to compete against IBM Corp. Knowles says Prime can successfully hold its own by controlling software applications packages, by offering products with greater compatibility, and by building on the company's technical reputation. *–Craig D. Rose*

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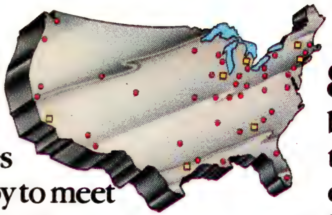

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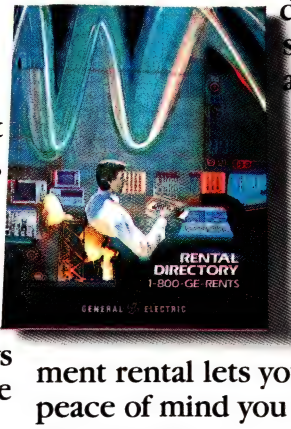

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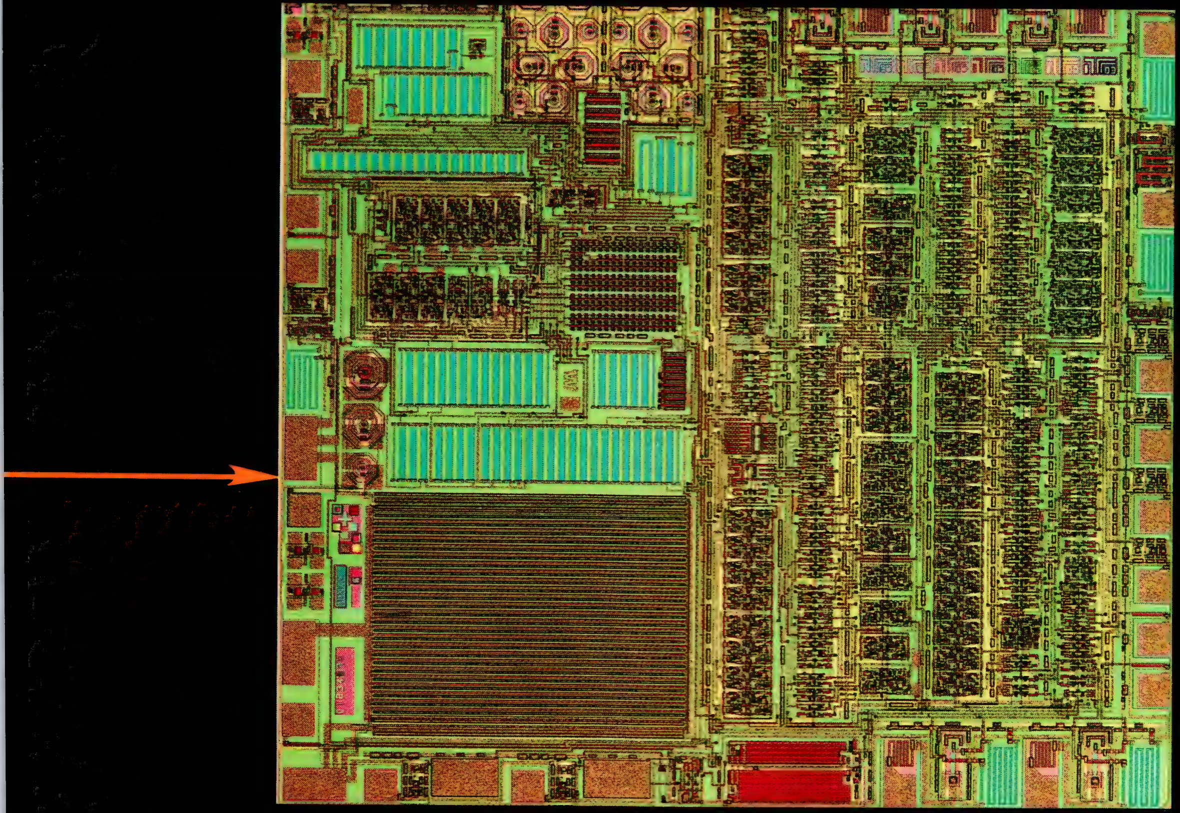

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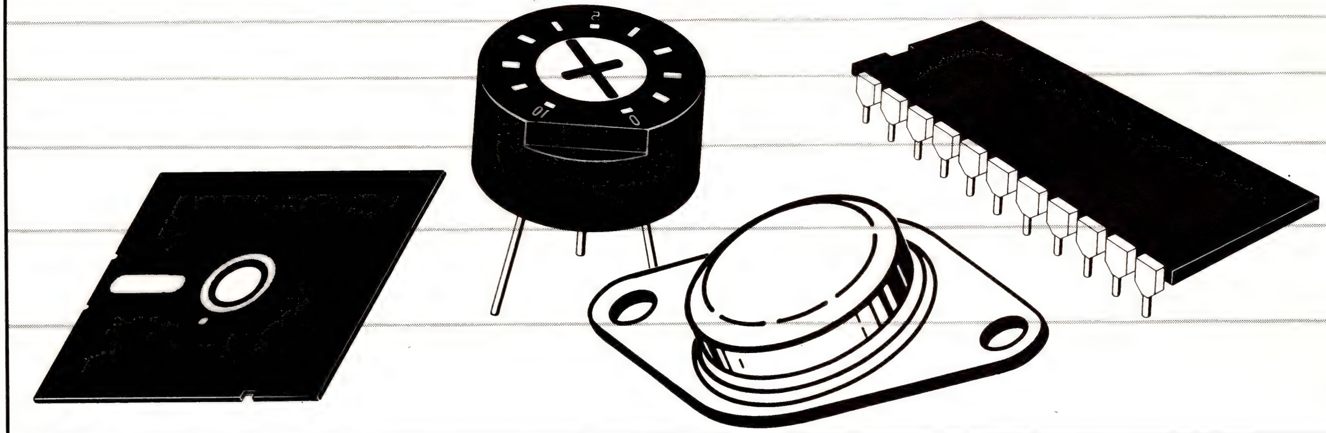

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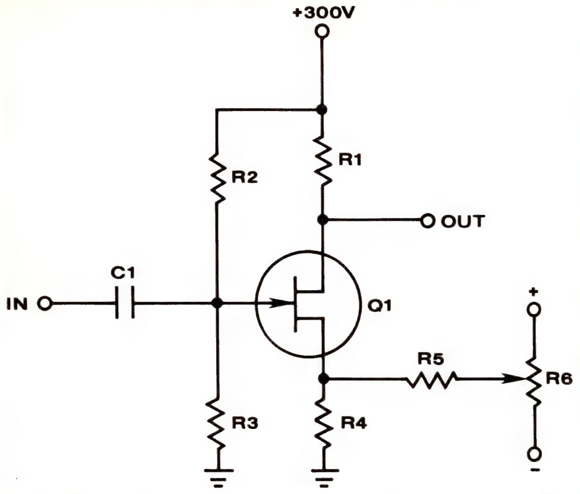

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HP TRIES TO GET ITS CAE ACT TOGETHER

NEW STRATEGY RELIES ON UPCOMING LINE OF INTEGRATED PRODUCTS

by Eve Bennett

FORT COLLINS, COLO.

Hewlett-Packard Co., well aware that it is late in coming to market and has a lot to prove, is about to redefine its presence in computer-aided engineering and manufacturing.

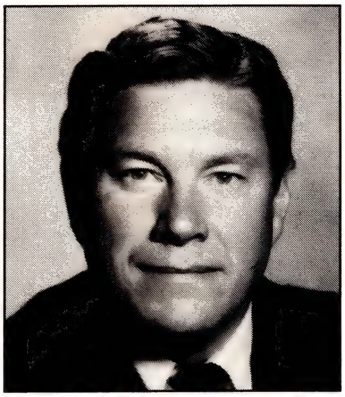
Until now, the company offered individual products, but without an overall market strategy. Now it is striking out in a new direction in CAE by integrating design, analysis, manufacturing, and testing, and is coming out swinging with a batch of coordinated CAE products. Also playing a role is newly acquired system-maker Cericor Inc.

HP's strategy, called DesignCenter, is initially to base a variety of products on its existing HP 9000 work stations, then on its newly announced Vectra, an IBM Corp. Personal Computer AT look-alike, and eventually on the reduced-instruction-set computers that will emerge from HP's Spectrum program. The first products under that plan, from HP's year-old Design Systems Group in Fort Collins, are the ME Series 5, 10, and 50 of computer-aided-design and CAM equipment for mechanical engineering.

Due for introduction at Autofact '85 in Detroit on Nov. 4-7, the ME Series ranges in price from about $18,000 for the entry-level Series 5, which performs two-dimensional drafting, to about $250,000 for the multiprocessor Series 50, which performs sophisticated solids modeling. Just how well these products and future CAD equipment will do in the marktetplace will depend on how well they meet the expectations that have been building ever since HP began reorganizing by establishing the Design Systems Group and its three business units, Workstation/Technical Computing, Electronics CAE/CAD, and Mechanical CAD/CAM. Also part of the group, as a partner to all the units, is the Technical Software Center, which does third-party software for engineering applications.

Some industry analysts, however, think HP's restructuring process has taken too long to produce too little. "Frankly, I'm underwhelmed," says David Wu of Montgomery Securities, San Francisco. "I'm not impressed with their hardware effort nor with their software effort."

Much of the analysts' disappointment comes from HP's delays in announcing new products. Vicki J. Brown, senior analyst with International Data Corp., Framingham, Mass., says she expected more software offerings at last year's Autofact. She says that despite HP's "very loyal customer base, they must pursue the end user, not just go after their existing base. HP really has to be aggressive." Though International Data ranks HP No. 8 in total CAD/CAE/CAM sales (table), it gives the company only a 3.5% share of a 1984 worldwide market it puts at $2.9 billion for U. S. companies plus another $1.2 billion for foreign players.



LEADER. William G. Parzybok Jr. leads the Design Systems Group, which coordinates 10 HP divisions.

HP concedes that there has been a delay. "It is late. We should have been in this business a long time ago," says William G. Parzybok Jr., vice president and general manager of the Design Systems Group, which coordinates the efforts of 10 HP divisions. "People wonder why HP isn't. [HP customers] think we can make a significant contribution."

Some observers expect an entirely new hardware platform. "I think they're waiting for the Spectrum hardware," comments Peter D. Schleider, a research analyst with L. F. Rothschild Unterberg Towbin of New York. He agrees that "it is still going to be a while before HP gets its CAE effort off the ground."

What HP is presenting now is a full set of software tools for mechanical engineering, developed both in house and elsewhere, which run on HP's mid- and upper-level 9000 series work stations. The sophisticated entrant is the ME Series 50, a CAD/CAM package for mechanical design, numerical control, and plastic injection

THE TOP 10 IN CAD/CAE/CAM WORLDWIDE SALES

Company	Revenue by application ($ million)					Total revenue
	Mechanical engineering	Electronic/electrical engineering	Architectural/electrical/civil engineering	Mapping	Services	
Computervision	272	111	56	6	111	556
IBM	391	13	16	—	109	529
Intergraph	64	20	178	89	52	403
Digital Equipment	107	103	22	32	37	301
Calma Corp. (GE)	70	90	28	—	47	235
McDonnell Douglas	94	—	24	—	16	134
Applicon	62	25	1	—	13	101
Hewlett-Packard	45	36	6	—	10	97
Control Data	54	7	9	—	23	93
Prime Computer	53	3	14	—	20	90

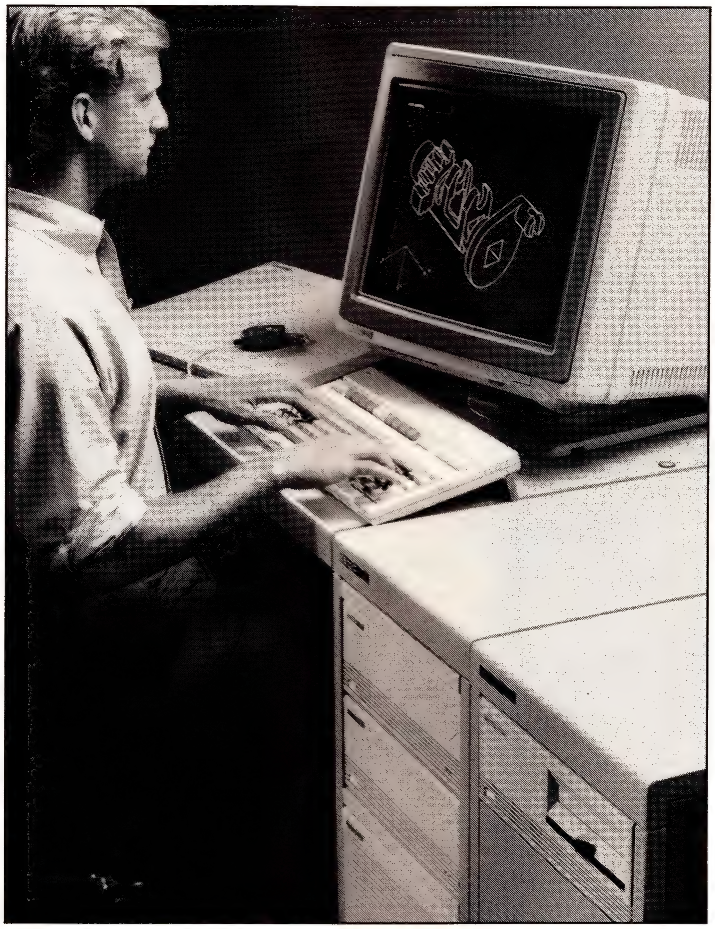
SOURCE: INTERNATIONAL DATA CORP.

molding. Residing on the HP9000 model 550 work station, it allows for 2-d and 3-d design and drafting, shading, and flat-pattern layout. Its solid-modeling design capabilities are based on a software core called Romulus, developed by Graftek Inc. of Boulder, Colo.

COMMON DATA BASE. The Series 50 software has a common data base for design and manufacturing. Geometric designs for manufacturing can be displayed dynamically in various formats that can give any combination of 3-d wireframe, surface representations, or solids modeling and edited interactively. Links also exist to analysis and testing. For example, at the analysis end, there is finite-element modeling with HP's direct support of Ansys, a general-purpose program that can deal with a wide range of engineering problems. It was developed by Swanson Analysis Systems Inc., Houston, Pa.

The entry-level ME Series 5 system for 2-d drafting is based on a 16-bit work station, the model 310. The ME Series 10 gives more advanced 2-d drafting and design capabilities and can link with the Series 50. Based on the 16/32-bit model 320 work station, it has a base price of about $33,000.

Jim Mosakowski, marketing manager for HP's Lake Stevens Instrument Division, admits "certainly it would have been more attractive if we had entered two to three years ago with these products."


MAKING ITS MOVE. The ME Series 50 is part of HP's DesignCenter—a series of CAD/CAE/CAM systems. The systems are based on the HP 9000.

Parzybok acknowledges that the new line will not be the answer to all customer needs. "Granted, we won't have some features when we first come out with these products. I'm not claiming we're going to blot out the sun."

HP is largely counting on its reputation with its customer base. "There's a large base of sentiment in our existing customers looking for us to succeed," says Mosakowski.

That concept—linking all the CAE products—is what HP terms the HP DesignCenter, not a place but a strategy for integration. Design Systems Group marketing manager Bill Watts says the DesignCenter approach gives HP a "more global view—we intend to make all of those tools work together."

From all levels at HP, the message is that if anything is the key to success it will be integration. No one else has provided a solution of comparable breadth and depth, Parzybok maintains, to the variety of HP and third-party software running on the various HP work stations.

The acquisition last month of Cericor, Salt Lake City, Utah, provides "a much more integrated environment with a very modern data base," Parzybok adds. The move also impresses analyst Schleider, who estimates the cost at $25 million to $30 million. "That's a major commitment to Cericor and CAE."

Cericor's current product is the CDA 5000, a sophisticated electronic design-automation system based on an artificial-intelligence language called Mainsail. It operates on a single integrated data base with an object-oriented architecture. This allows creation of the data base at the same time as the design.

Beth Tucker, a senior analyst at Dataquest Inc., San Jose, Calif., says products such as Cericor's are a major factor in the CAE market. She notes that the trend is toward central data bases that can allow for analysis "from a manufacturable point of view and from an interactive point of view."

A notable feature of the CDA 5000 is that it already runs on one RISC-based machine from Ridge Computers of Santa Clara, Calif., the Ridge 32. That feature makes it a particularly good addition since HP wants to ease the switch to its RISC-based Spectrum products as they emerge.

And Spectrum products are probably not too far down the line. John A. Young, president and chief executive officer of HP, recently stated that first Spectrum product announcements are planned for early 1986. In late August, when the HP 3000 Series 58 business computer was introduced, Young also said that "our commitment to protecting customer software investments remains a central goal of the Spectrum program—not only for future HP 3000 products but also for future high-end HP 1000 real-time systems and HP 9000 design systems."

As customers evaluate HP's current CAE products, they will be looking for more signs that the investments they make today can be upgraded. Parzybok says that "we feel we give the broadest possible range of solutions." To maintain that broad position, he says, some CAE systems will be offered on the Vectra this year.

The market, at least that segment made up of loyal HP customers, will also be looking to the new CAE systems for electrical engineering design, where HP's historical strength lies. An indication of HP's direction there is its just-announced marketing agreements with some of the leading suppliers for printed-circuit-board and IC-design software.

HP has signed with FutureNet Corp., Chatsworth, Calif., a Data I/O Corp. subsidiary and maker of IBM PC-based CAE tools, for its DASH schematic design and documentation package; Analog Design Tools Inc., Menlo Park, Calif., for its Analog Workbench, one of the few packages for analog circuit design; Zuken Inc. of Tokyo, the largest pc-board CAD vendor there, for its System 2000; as well as with VLSI Technology Inc., San Jose, Calif., a producer of tools for application-specific IC design.

Though there might be disagreement among market watchers about the quality and quantity of HP's new products, there can be no doubt that the company, whose total sales this year will reach an estimated $6.6 billion, means to improve its ranking in CAE sales. ☐

SHORTAGE OF OBSOLETE CHIPS MAKES IT TOUGH ON MILITARY

MAKERS CALL FOR STANDARDIZATION TO SOLVE GROWING PROBLEM

by George Leopold

WASHINGTON

The dramatic growth in leading-edge semiconductor technology has spawned one unforeseen and troublesome consequence: parts rapidly become obsolete and hard to get—especially for the military. Chip makers drop older products in favor of new, more profitable lines as they scramble to serve the commercial customers that account for nearly 90% of their business. This leaves buyers of military electronics systems—some designed to last up to 30 years—hard up for replacement parts.

"In the semiconductor industry, Uncle Sam is the low man on the totem pole," laments one Defense Department official. The problem has worsened, even during the current industry downturn, when the military market grew as other sectors foundered. The U. S. market for discontinued parts is estimated to be $15 million a year. But both industry and the military are giving the problem an increasing amount of attention.

One sign of that concern is that for the first time a separate technical session on discontinued parts will be held at this year's Government Microcircuit Applications Conference, Nov. 5-7 in Orlando, Fla. Participants will discuss such potential solutions as designing standardization into military systems, emulating microcircuits, and finding substitute parts that can fill in for the ones specified. Elsewhere, such forums as the Semiconductor Industry Association's Government Procurement Committee are beginning to bring suppliers and end users together to grapple with the problem.

The shortage of parts has been a concern for several years, but it has now become critical, explains Herbert L. Mette, of the U. S. Army's Electronics Technology and Devices Laboratory at Ft. Monmouth, N. J., and technical program chairman of the conference. Mette, who was instrumental in getting the session on the program, asserts that semiconductor manufacturers are "dropping lines massively, and we are left holding the bag."

Government contractors, as well as the military, are feeling the pinch. Manufacturers are announcing "last runs" for entire product lines with alarming frequency, says conference participant Leonard M. Pauplis, product assurance manager for GTE Government Systems in Needham Heights, Mass. Meanwhile, government procurement agencies have been issuing alerts to contractors on scores of discontinued IC types, he says.

Although the problem of discontinued parts goes back to vacuum tubes in the 1960s, it started getting serious when MOS technology came into widespread use about five years ago. Another factor was a decision several years ago by IC manufacturers such as Motorola Inc. and Fairchild Camera & Instrument Corp. to discontinue production of 5400-series devices used in military systems for the past 20 years, explains session participant Richard A. Lane of the U. S. Army Missile Command at Redstone Arsenal, Alabama. Now that the parts pipeline has dried up, that decision is having a major effect, Lane says.

Uncle Sam is left 'holding the bag' as makers drop lines

Many observers blame the semiconductor industry for concentrating only on leading-edge technology for the commercial sector. But James Asher, vice president of commercial relations and administration for Melbourne, Fla., chip maker Harris Corp., doesn't agree. He says that indiscriminately dropping military product lines just doesn't make good business sense. "I think it's a bad rap on the [IC] industry."

NO EASY ANSWERS. "This is one of those problems where there is no easy answer or a totally satisfactory answer," says Asher, a member of the SIA's Government Procurement Committee, which is assessing government end-user programs. Government agencies and contractors, trying to determine how many parts they will need for a "lifetime buy," have complained about inadequate notice when a part is discontinued. The customers' inability to predict the length of a program or the number of systems to be built is "the biggest single problem" for suppliers of obsolete parts, Asher says.

One solution to the problem is to design standardization into military systems, declares another SIA committee member, James Houlditch, a senior vice president at Texas Instruments Inc. One of his committee's primary functions is to encourage government agencies, such as the Defense Electronics Supply Center, as well as original-equipment manufacturers to buy standard parts as a way of ensuring adequate supplies.

Partly in response to industry's call

MILITARY PRODUCTS' MARCH TO OBSOLESCENCE

Design-in and preproduction	Growth	Maturity	Decline	Phase-out
• Gallium arsenide • Very high-speed IC program • 32-bit CPU • MOS 256-K DRAM • CMOS universal programmable UP logic	• Schottky transistor logic • Advanced Schottky/ Fast TTL • Programmable array logic • Advanced low-power Schottky • EEPROM • CMOS static RAM • Bipolar PROM • MOS 64-K DRAM • 9989	• n-MOS UP logic • Bit slice • n-MOS EPROM • Linear ICs • Opto-electronics • Bipolar RAM • Low-power Schottky • TTL • Schottky TTL	• Emitter-coupled logic 10-K • TTL • MOS 16-K DRAM • Microwave • High-speed TTL • Power discretes • Small-signal discrete	• Low-power TTL • Diode-transistor logic/ Sylvania universal high-level logic • Beam lead

SOURCE: ROCHESTER ELECTRONICS INC.

for standardization, the Pentagon has launched a military drawing initiative to reduce the number of source-control drawings available for military systems. Currently, from 4,000 to 5,000 unique IC designs and about 10,000 separate part numbers are available to designers of military electronic systems.

With drawings costing between $8,000 and $10,000, the initiative "should be able to save at least one third of that right off the bat," says Edmund J. Westcott, deputy chief of staff for product assurance and acquisition logistics for the Air Force Systems Command, Andrews Air Force Base, Md. The initiative would provide standardization. "We believe that people can design systems with building blocks. We don't need the proliferation we've had before."

Other fronts have seen action too. An eight-phase program called the Microcircuits Emulation Program was established in 1983 as an alternative to lifetime buys from suppliers. "The ultimate goal is to give the DOD the capability to emulate out-of-production semiconductors," explains Dudley W. Caswell of the Defense Logistics Agency's Office of Plans and Policy in Alexandria, Va.

One solution: cut the number of parts available to designers

The first phase of the 12-year program, for which contracts have yet to be awarded, would focus on bipolar technology emulation and attempts to integrate six or seven processes on one wafer. Later phases would explore MOS emulation, gallium arsenide, and cross-processing using different technologies.

The notion that discontinued parts can be replaced through microcircuit emulation is also the subject of one of six papers to be presented at the Gomac technical session. The paper, submitted by the Naval Ocean Systems Center in San Diego, explores three different emulation approaches and argues that newer fabrication techniques such as plasma etching and ion implantation can be used to provide "form, fit, and function" replacements.

COSTLY REDESIGN. But one of these approaches, emulation through redesign, is too costly to serve as a new source of discontinued parts, say some observers. GTE's Pauplis calls redesign the "option of last resort." Richard Lane of the Army Missile Command agrees: "It's extremely costly. The last thing you want to do is redesign."

If the time and money necessary for a redesign are lacking, says Pauplis, a lifetime buy—the most common alternative—makes sense. But the manufacturer must know the total quantity needed. If quantity cannot be determined, Pauplis favors use of substitute parts, which he says cost no more than the original parts and have a minimum effect on the assembly and shipment of equipment and spares. And a handful of companies that distribute obsolete parts are even making a profit (see "Making a business out of obsolete parts").

Attention to the discontinued-parts problem will not end with Gomac. The following week, the SIA's Government Procurement Committee will pick up where Gomac leaves off. Made up of key industry executives, the committee has scheduled a meeting with government officials to work on such issues as standardization and alternate sources.

Westcott of the Air Force will be a key player at the meeting. Although he differs with industry on issues such as adequate notice on discontinued parts, Westcott remains conciliatory. "We want to work with the device community to get the best availability." □

MAKING A BUSINESS OUT OF OBSOLETE PARTS

As the Pentagon scrambles to fill the gap created by diminishing sources for obsolete parts, a new type of supplier specializing in these discontinued parts has sprung up. One of the biggest is Rochester Electronics Inc., which currently maintains an inventory of more than 40 million parts. Another company, Lansdale Transistor and Electronics, will even manufacture as well as distribute obsolete parts.

Curt Gerrish, president of Rochester Electronics, founded the Wakefield, Mass., company in 1982 after putting in 16 years at Motorola Inc., where he was a vice president for distributor marketing. He still represents Motorola in New England for maintenance and repair. Gerrish also has agreements with Texas Instruments Inc. and Fairchild Camera & Instrument Corp. to distribute their discontinued 5400- and 7400-series logic devices.

Fairchild, for example, is shipping him another 2.76 million parts. "We buy everything left after the end of life [of a product], from wafer to specials, and other finished products," Gerrish says. The privately held company does about $2 million a year in business. Even major electronic-component distributors have expressed interest, he says. The U. S. market is estimated to be about $15 million a year.

Gerrish apparently provides a much-needed service during the current shortfall in parts for military electronics systems. "We receive regular emergency phone calls from various government agencies, military subcontractors, and a wide range of other users," he says.

The semiconductor industry veteran doesn't mince words about the parts shortage. Gerrish bemoans what he calls the industry's "indifference to the older product lines." He also maintains that "the engineers who run the business are only interested in new products." And despite the existence of such industry groups as the Semiconductor Industry Association's Government Procurement Committee, the industry would sooner destroy obsolete parts than correct the problem, he says.

Gerrish is putting his money where his mouth is. By year end, he expects Rochester Electronics to move into a new and bigger facility in Newburyport, Mass. The new operation will have computerized inventory control and will be able to package dice.

At Lansdale Transistor and Electronics, an agreement has been signed with Motorola's Semiconductor Products Group to acquire the manufacturing and marketing rights to Motorola's Sylvania Universal High-Level Logic line. The high-level line is a forerunner of common TTL, still used in military systems designed in the 1970s.

Motorola will transfer the entire mask, assembly, test, and burn-in tooling, plus its remaining inventory of Sylvania high-level logic parts, says R. Dale Lillard, president of Lansdale. Lansdale purchased Signetics Corp.'s obsolete line of TTL and diode-transistor logic in 1983.

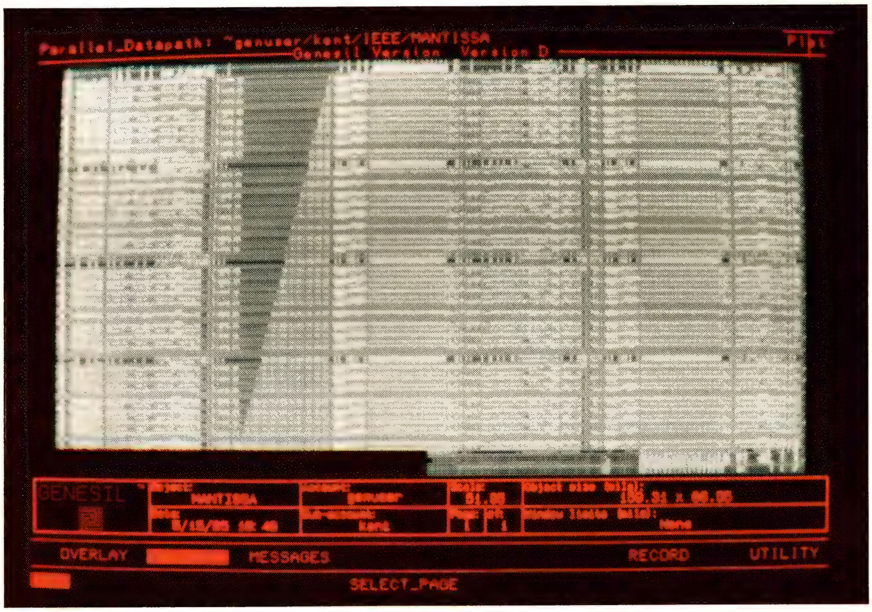
A division of Electronic Technologies Inc., Phoenix, Lansdale was formed to market germanium transistors purchased from Philco in 1964 and Motorola in 1976. It entered the market for obsolete integrated circuits in 1980. "We're marching up the back side of the bell curve," explains Lillard.

With a staff of 90, the company will concentrate on 5400-series products for the military as manufacturers drop their lines, he says. But he can't predict what will follow. With product life cycles getting shorter, Lillard predicts that it won't be long before Lansdale will be producing 256-K dynamic random-access memories.

WHY SILICON COMPILERS HAD TO CHANGE ITS STRATEGY

INTRODUCING THE GENESIS TOOL KIT TO GET IC DESIGNERS ON BOARD

by Jeremy L. Young



SHOWING THE WAY. The Genesil silicon compiler, built by Silicon Compilers Inc. for system designers who want to do their own VLSI, uses a data-path compiler to lay out a circuit.

SAN JOSE, CALIF.

Silicon Compilers Inc. has learned that it is hard to sell its year-old Genesil integrated-circuit design system without the backing of the people who design ICs. So to settle this quandary, the company is introducing Genesis, which is targeted at those very IC designers, as a means of getting them to endorse Genesil.

The original intent of Genesil was to allow those of the more than 300,000 systems designers who want to bypass the 4,000 or so very large-scale IC experts to design their own ICs. Genesis is a new set of tools for developing silicon-compiler modules that can be put to practical use only by the same small band of IC designers the company sought to avoid in the first place.

The new set will be unveiled at this week's Automated Design and Engineering for Electronics show in Boston (see Technology to Watch, p. 50). The system consists of a suite of specialized languages for writing block or function compilers, programs for verifying the correct function of those compilers, an interface to Calma Co.'s GDS II chip-layout systems, and other tools.

Clearly, Silicon Compilers doesn't expect business from Genesis to cause a big bulge in its bottom line; there are too few IC designers to make up a substantial market. But that exclusive brotherhood of semiconductor specialists is a pivotal group at this point in the history of compilation technology. Genesis represents Silicon Compilers' first major attempt to pull as many of these influential IC designers as it can aboard the silicon-compilation express.

The plan: Genesis will spur sales of Genesil compiler

The reason for the new strategy is that the market for silicon compilers is not growing as fast as the company projected it would when it launched its first products, just when the current slump in the computer and semiconductor industries was beginning. There is also competition in the form of silicon-compilation products from newer startups such as Seattle Silicon Technology and Silicon Design Labs Inc. Thus Genesis is expected to go a long way toward encouraging sales of the company's bread-and-butter Genesil systems.

Then, too, Silicon Compilers hopes the support of IC designers gained through their use of Genesis will help the company establish the credibility of its technology, which should boost Genesil sales.

The company also hopes to get help from outside IC experts in expanding the number of compiled functions that it can offer, thereby increasing the number of applications that Genesil can address.

Sales of Genesil systems are some 30% to 40% behind the business plan Silicon Compilers mapped out just over a year ago, according to Stephen C. Johnson, vice president of product development. The company says it has installed more than 70 Genesil designer stations. Some are single-user configurations running on Digital Equipment Corp. MicroVax II hardware, and some are terminals connected to larger multiuser VAX systems. The company has 30 to 40 customers; on the average, each has purchased capability for two designers.

The company points to current market conditions in the industry to explain the sales shortfall. But it also faces natural and healthy skepticism about its radically new design methodology.

When Genesil first came to market, "it wasn't obvious to us that every systems engineer knew an IC designer," says Johnson. When systems designers turn to their trusted IC associates to ask them if a computer can design a good chip, they do not often come away reassured, Johnson admits. He notes that Genesil's detractors are making the same mistake that computer programmers working with assembly language made back in the 1950s when they questioned the usefulness of the first compilers for high-level languages.

"When we first talked to [IC designers at] the semiconductor companies, they said, 'Until I know how you guys do it—in excruciating detail—I won't believe it. It's still a black art to me,'" says Dennis Sabo, Silicon Compilers' vice president of sales and marketing.

"We needed to open our kimono to them so they could see that our system is based on solid engineering. Genesis gives our product family the openness the semiconductor people want."

Nothing could illuminate the operation of Genesil more clearly than letting users write their own block compilers for it, which is what the Genesis system makes possible. And no technology gives the IC specialist anything approaching the design leverage he gets by writing modules for a silicon compiler, says Johnson. Semiconductor houses searching for ways to capitalize on the expertise of their people cannot afford to overlook silicon-compilation technology, he thinks.

If Silicon Compilers can convince IC designers at semiconductor companies and large systems vendors to start writing function compilers, it may be able to expand the library of functions it can offer to customers. "The breadth of the system's applicability is directly proportional to the number of compilable functions available," says Sabo. More than 50 circuit functions are supported already, but "it's no longer the RAM or ROM compiler. It's 'let's have an 8051 compiler, or a 2900 compiler,'" he says, referring to two popular microprocessor families.

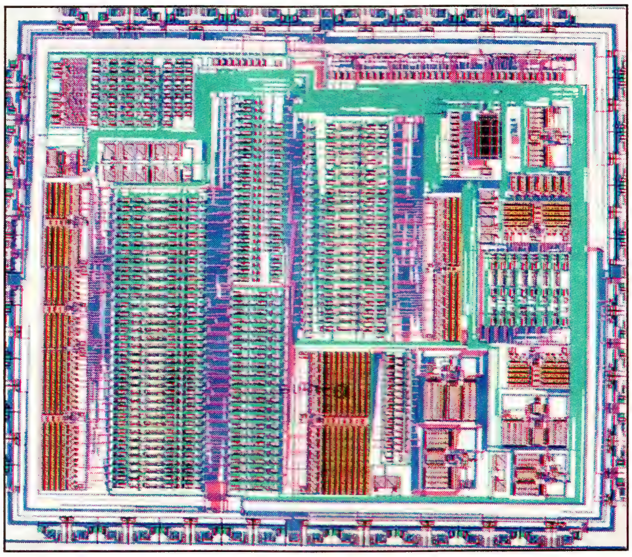
Users need incentives to release their own function compilers for use by other Genesil customers, some of whom may be their direct competitors. To provide those incentives, Silicon Compilers is setting up what it calls the Genesil Function Provider program.

DISCOUNTS. The first motivation it provides is a major discount on the price of a Genesis system. The tool set sells for $60,000 as an add-on to a Genesil system. The base price for a single-user Genesil system, including the MicroVax II hardware, is $165,000. A stand-alone Genesis system, which includes a subset of the Genesil functions, will sell for $125,000, including a MicroVax II engine. Customers who enter the Function Provider program get an immediate discount of $30,000 on the price of Genesis.

To get the discount, a customer must pledge to make available to Silicon Compilers within the next 12 months one function compiler that does not duplicate capabilities Genesil already offers. Silicon Compilers may then distribute that function compiler to other customers, without anyone paying royalties or other fees to the customer that developed it. The 12-month time frame will be flexible, says Sabo.

The company is also considering other types of incentives. One possibility is to offer a special group of function compilers it has developed to participants in the Function Provider program at substantial discounts in return for additional contributions to the library of functions available to all customers.

To succeed in such a cooperative program, Silicon Compilers must maintain very constructive working relationships with its customers. A recent indication of success in this area was the announcement late last month of an agreement with one of the early Genesil users, General Dynamics Corp., the giant St. Louis defense contractor [*Electronics,* Sept. 30, 1985, p. 27]. In return for help in applying silicon-compilation technology, General Dynamics will work with Silicon Compilers to help it understand the special requirements of defense work. In addition, General Dynamics has invested $4.2 million to acquire a 5% interest in the San Jose company.



TIGHTLY PACKED. Digital signal processor designed by Seattle Silicon compiler claims a device density of 1.25 mil^2 per transistor.

Silicon Compilers has been pleasantly surprised by the amount of interest the military community has shown in its technology, says Sabo. The company's involvement in military work deepened last month when the Department of Defense accepted a contract proposal that the company made in conjunction with the Research Triangle Institute and E-Systems Inc., Dallas, to develop an interface between Genesil and the Pentagon's VHSIC (Very High-Speed Integrated Circuits) Hardware Description Language, or VHDL. This will permit Genesil users to implement circuits that have been described using VHDL for design-phase simulation.

General Dynamics likes Genesil, invested $4.2 million

Another part of the job will be to calibrate Genesil for use with one of the process technologies developed under the VHSIC program. Although Silicon Compilers is not yet tackling the bipolar VHSIC process, it has agreed to tune its system to produce tapes for the 1¼-µm double-metal CMOS process developed under VHSIC.

Though the calibration work is not due to be completed until the end of 1986, military customers are already coming to Silicon Compilers to begin design work, says Sabo. They can design chips on the current version of Genesil, and when the 1¼-µm technology files are ready, hit the button to produce mask tapes. Silicon Compilers also has a contract to calibrate the Genesil system to National Semiconductor Corp.'s VHSIC-process foundry.

Another major partnership, though not a military one, was announced last week between Silicon Compilers and General Electric Co., Fairfield, Conn., parent of Calma. GE has been moving to grab some application-specific-IC business with gate-array products, standard cells, and now silicon compilation. Genesil systems are to be made available to customers at two GE design centers.

"The standard-cell business has not picked up during the last five years the way people thought it would," says Sabo. GE is responding to that fact, he says, and will recompile its standard-cell functions using Genesil. Silicon Compilers will calibrate Genesil to produce tapes for GE's 2-µm double-metal CMOS process as well as for its 1¼-µm advanced VLSI double-metal CMOS process.

Such announcements go a long way toward establishing the credibility of the Genesil technology with systems engineers. But in deciding to offer the Genesis tools, Silicon Compilers has been influenced by factors other than the need for more credibility. For example, Silicon Design Labs, Liberty Corner, N. J., last May introduced its generator-development tools (GDT), a package aimed at the same group of users—IC designers—and essentially the same task [*ElectronicsWeek*, May 20, 1985, p. 21].

GDT includes a language developed to write function compilers, or generators, as Silicon Design Labs calls them. Silicon Compilers' Johnson claims that Genesis' connection to Genesil tools provides a number of added capabilities. Genesil offers a consistent set of data structures and language features that provide links to a suite of analysis tools. A function compiler written in Silicon Compilers' languages produces designs that can immediately be put through functional and timing simulations and a program that estimates the amount of power the circuit will use.

These capabilities, which GDT does not offer, give the compiler user a lot more useful feedback for the iterative design process, Johnson maintains. And the Genesis interface to GDS II lets designers use their existing Calma layout-design systems instead of investing in the new layout hardware and software that GDT uses and devoting the time it takes in learning to use it.

Yet another language for writing circuit-function compilers is available to selected customers from Seattle Silicon Technology, Bellevue, Wash. Called SLIC, short for silicon language for integrated-circuit layout, it is used by the company to write modules for its Concorde function compilers.

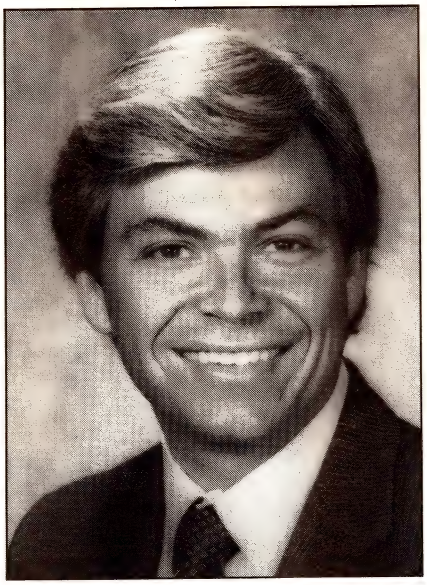
Instead of developing a complete environment like Genesil, Seattle Silicon chose to write functions for its Concorde compiler that work with the software tools already running on design work stations from Valid Logic, Mentor Graphics, Tektronix, and CAE Systems. In addition to module compilers, Seattle Silicon offers other tool sets designed to fit within the work-station environment.

At the ADEE show this week, it will introduce two interconnect routers that tie compiled modules together on a chip. One of these reduces a job—routing an IC with about 25,000 transistors—that took 22 hours with the company's older router to a quick 4 minutes, says Gordon Kuenster, president.

Seattle Silicon has introduced competing system

OP AMPS, TOO. Unlike Silicon Compilers, Seattle Silicon offers compilers for such analog functions as operational amplifiers and data-acquisition circuits. Kuenster says that one third to a half of his customers—he refuses to reveal how many there are—want these analog functions. Another advantage he claims for his company's approach is that it permits the user to simulate circuits Concorde generates within the context of the circuit board or system in which the chip is intended to operate.

Silicon Compilers' Sabo calls the Seattle Silicon approach "a half step toward silicon compilation." He says these cell compilers lack the underlying framework of an overall design methodology, making it impossible to ensure that the complete chip is designed consistently. More chip expertise is needed to weave together the compiled modules, and "we don't think that's going to work for systems engineers at all," he says.



SELLING TOOLS. IC designers were skeptical at first, says Dennis Sabo, Silicon Compilers' vice president of sales and marketing.

The Genesil system, he goes on, does offer that underlying framework. It produces consistent data structures and modules; its circuits conform to a clocking strategy that provides avenues for adding asynchronous signals without disrupting the rest of the design.

Other underlying strategies have been developed for power busing, bonding-pad design, routing, fabrication-line calibration, and layout standardization. Furthermore, Johnson points out, cell compilers that simply produce a layout file do not offer the rapid feedback that Genesil does concerning a compiled circuit's speed, power requirements, and functionality.

Genesis, on the other hand, can be seen as a way to entice practitioners of the cell-compiler art into Silicon Compilers' camp. With Genesis, users can write block compilers very similar to those of Concorde and use them simply for generating circuit layouts. But the door is left open to bring the block compilers written with Genesis tools back into the Genesil environment, when and if the user sees an advantage in doing so.

One key area of competition among silicon compilers is in how efficiently they use silicon.

Silicon Compilers offers as an example a device density of 2.14 mil^2 per transistor for a computer-peripheral-chip design that one of its customers completed last month. The single-metal n-MOS chip, which uses 2-μm design rules, measures 45,242 mil^2 and carries 21,188 transistors. (The company says that chips two and three times that size have been designed with Genesil, and that most activity is now in denser double-metal CMOS technology. This capability was shipped in July.)

Seattle Silicon claims a substantially better device density of 1.25 mil^2 per transistor for the digital signal processor that E-Mu Systems Inc. of Santa Cruz, Calif., developed with Concorde for a music synthesizer. The all-digital IC, generated mainly with a data-path compiler, is about 62,500 mils^2 in area and carries some 50,000 transistors. The CMOS technology used has 2-μm design rules and two layers of metal.

Aiming to increase compilers' ability to use silicon efficiently, Micropower Systems Inc., Santa Clara, Calif., has developed a new 2-μm CMOS process that offers not two but three layers of metal interconnections, two of molybdenum, and a top layer of aluminum. This gives the compiler more degrees of freedom during routing so that it can produce chips that compare in density to hand-crafted ICs, according to the company.

Silicon Compilers, Seattle Silicon, and Silicon Design Labs are all relatively young companies that are focusing their efforts on compilation technology. Compilation has also been introduced as an added component to more mature design-automation systems, essentially as an adjunct to the standard-cell approach.

VLSI Technology Inc., San Jose, Calif., is one company that has been doing this for some time. Most of its ASIC designs are done with gate arrays and standard cells, but it claims to have completed more than 200 chips for customers using cell compilers. The company says it has compilers that fit in 45 categories, including arithmetic-logic units, programmable logic arrays, memories, and n×n multipliers. Last summer it added new compilers for general logic and data paths based on the 2901 architecture of Advanced Micro Devices Inc., Santa Clara, Calif.

Standard-cell vendors are adding compilers

Britain's Plessey Co. plc last month introduced a similar type of capability for its Megacell design system [*Electronics,* Sept. 30, 1985, p. 20]. Megacell combines Microcells—small glue-logic cells—with very large standard cells called Supracells and programmable cells called Paracells.

Chipsmith, a silicon compiler from Lattice Logic Ltd., Edinburgh, Scotland, has been used by Ferranti Semiconductors, Oldham, England, to process logic designs for six major contracts. Ferranti says 10,000-gate chips are achievable using 2-μm feature sizes. ☐

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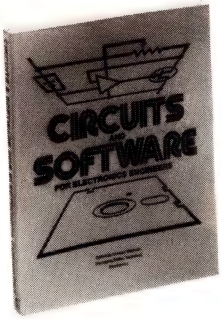

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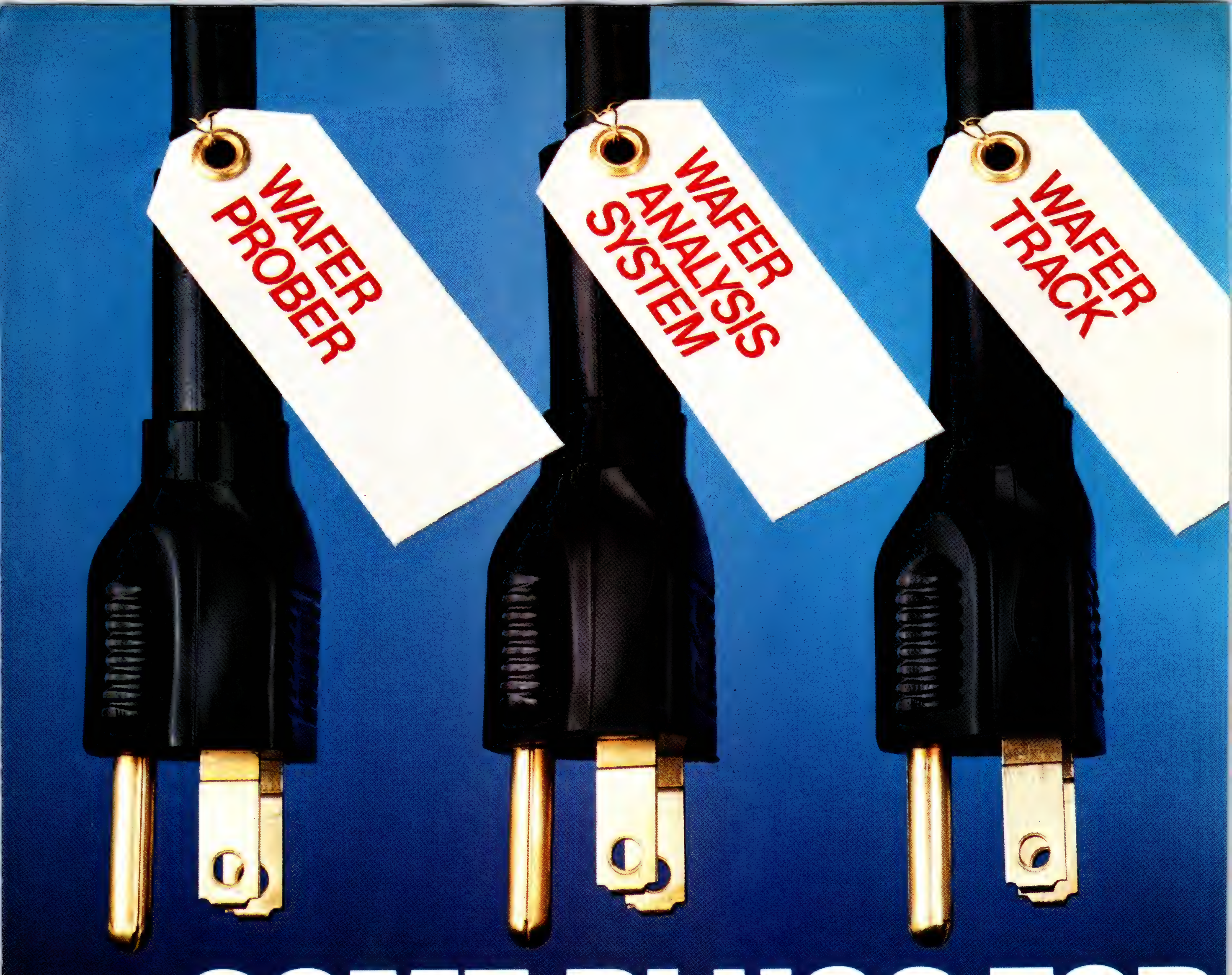

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HERE COMES A DO-IT-YOURSELF SILICON COMPILER

DESIGNERS CAN PLUG IN THEIR CIRCUIT KNOWLEDGE TO DESIGN CHIPS

When silicon compilation emerged as a concept in the early 1980s, it seemed just the ticket for struggling chip designers working on ever more complex integrated circuits. Created by Dave Johannsen, then a graduate student at the California Institute of Technology under Carver Mead, silicon compilation became a product late last year: Silicon Compilers Inc., cofounded by Johannsen, introduced Genesil, a program developed by him that enabled systems designers to create very large-scale ICs from high-level functional descriptions.

TECHNOLOGY TO WATCH is a regular feature of *Electronics* that provides readers with exclusive, in-depth reports on important technical innovations from companies around the world. It covers significant technology, processes, and developments incorporated in major new products. The reports also analyze technical data so that readers can assess the impact of new developments. The key people on the Genesis project at Silicon Compilers Inc. were Dave Johannsen and Jim McBeath. Karel J. Kosman, founder of Raycom Systems Inc., developed simultaneous bidirectional communications on a single optical fiber.

So far so good. But the program had a major flaw: IC designers couldn't use their circuit-design knowledge and techniques with Genesil. So it was back to work for Johannsen. Now 29 and vice president of advanced development, Johannsen has just led the development of the Genesis silicon-development system, which does what Genesil couldn't and wasn't meant to do. It is the first program to create silicon-compiler systems complete with analysis modules, such as Genesil, for IC designers.

While Genesil is a set of parameter-driven expert systems for circuit synthesis and analysis, Genesis is a set of development tools that VLSI engineers and designers can use to create silicon-compiler systems. Several systems manufacturers are already using the Genesil silicon-development system. And the silicon-compiler-system design methodology has sparked the interest of the IC-design community because of its potential for better circuits and faster turnaround.

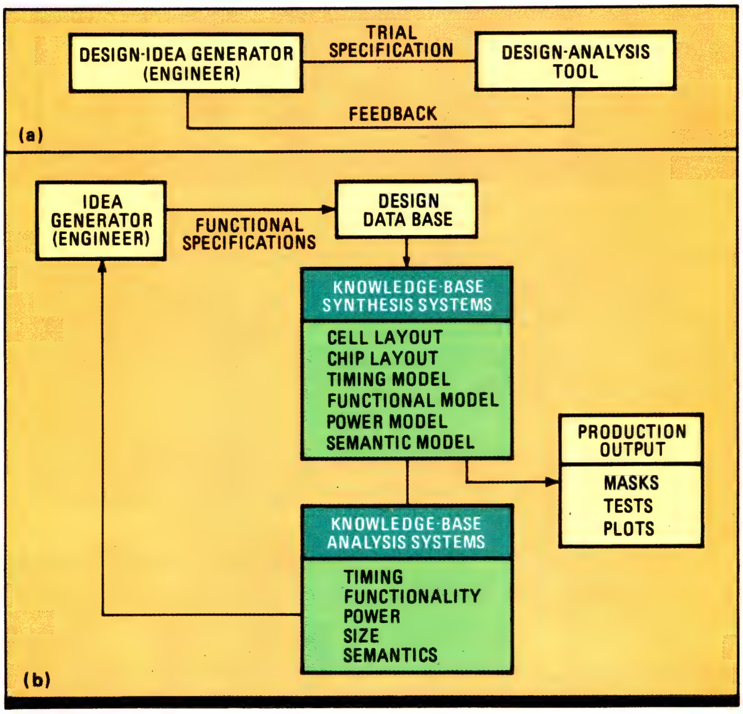
Systems designers are usually happy with the design methodologies built into Genesil. But VLSI designers often want to incorporate their own strategies in areas such as global design, power distribution, floor planning, and interconnection. With Genesis, an open system containing all Genesil's synthesis modules, they can apply their own techniques for circuit design, layout, and packaging.

The products give designers two choices. They can use Genesis to build complete compiler systems by creating their own compilers and analysis modules. Or they can build on Genesil's IC-design expertise by acquiring both Genesis and the Genesil compilers and analysis modules and using Genesis to add to the Genesil vocabulary.

A silicon-compiler system's vocabulary consists of the circuit functions that it can synthesize and analyze. A large vocabulary is important to IC designers because the utility of a design-aid system is often proportional to the size of its vocabulary.

For example, designing a digital signal-processing chip will probably require a digital-filter-circuit building block. To build a digital filter requires a multiplier circuit. If the compilation system has no multiplier, the designer must create one from other functions. Such a compiler system is not as useful as one with a multiplier in its vocabulary. Though this is a simple example—any compiler worth its salt would have several kinds of multipliers—it shows that the richer a compiler's vocabulary, the better the system is.

The ideal design method is one in which "the engineer receives instantaneous feedback about all pertinent details of his proposed design, thus permitting rapid convergence on the best solution," says Stephen C. Johnson, vice president of engineering and product development at Silicon Compilers. In essence, design is by successive refinement (Fig. 1a).

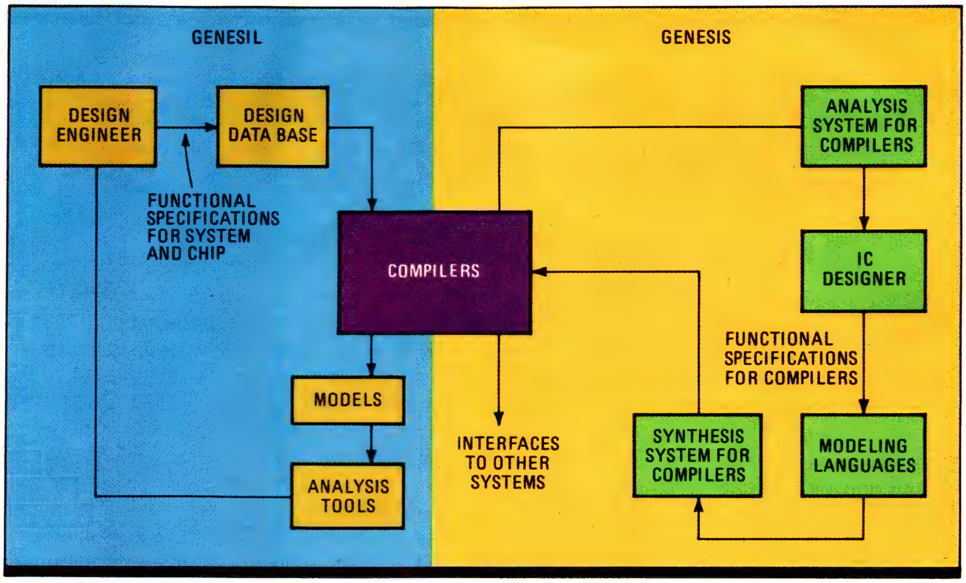


1. IDEAL DESIGN. In an ideal design process, engineers generate specifications, and a design and analysis system comes back showing the circuit's important characteristics (a). Silicon compilation provides this flow (b).

In IC design, only four types of feedback are required—power-dissipation information, timing performance, functional verifications, and size information. Silicon compilation supplies this feedback in minutes, so designs can be completed much more quickly and designers can try more options. The result is better IC designs in a lot less time. "For example, a 75,000-transistor circuit might take 450 man months to design by the old conventional method, 350 man months if just cell compilation is used, but only 18 man months with complete silicon compilation," says Johnson.

Cell compilation (or block compilation) is the part of silicon compilation that synthesizes the layout of a portion of a circuit. But it does not produce models that analyze function, power, and timing: the only immediate feedback an engineer gets from cell compiler is the size of the circuit, not the power, timing, and function information. Cell compilers also do not give help in arranging and wiring the blocks that have been compiled, as a complete silicon-compilation system will.

Genesil closes the loop in the ideal design flow. The analysis and verification steps with their attendant feedback are just as important as the circuit-synthesis functions. Genesil includes knowledge-base expert systems that do both synthesis and analysis. It has expert systems for generating models of cell and chip layout, timing, functionality, power, and semantics. The same expert systems can interpret these five models and provide data feedback which the engineer can use to determine if the circuit is what he wants (Fig. 1b). If it is not what he wants, he changes a few things in the functional description and sends it around the compiler-system loop again.


GENESIL
GENESIS
DESIGN ENGINEER
DESIGN DATA BASE
FUNCTIONAL SPECIFICATIONS FOR SYSTEM AND CHIP
COMPILERS
MODELS
ANALYSIS TOOLS
ANALYSIS SYSTEM FOR COMPILERS
IC DESIGNER
FUNCTIONAL SPECIFICATIONS FOR COMPILERS
INTERFACES TO OTHER SYSTEMS
SYNTHESIS SYSTEM FOR COMPILERS
MODELING LANGUAGES

2. BOTH SIDES. The Genesil side of Silicon Compilers' silicon-development system provides the compilers and design environment for system engineers; the Genesis side is for generating compilers.

The Genesis tool set lets designers create full-function compilers to install in Genesil. These extend its vocabulary by providing access to Silicon Compilers' programs for synthesizing and verifying compilers. In addition, Genesis permits the design of stand-alone Genesil-independent compilers. Another potential benefit of the Genesis system is that it could become a de facto silicon-compilation standard, if enough IC designers use it.

WHAT'S INSIDE?

The Genesis part of the combined Genesil-Genesis extendable silicon-development system includes a compiler-analysis system, compiler-synthesis system, modeling languages, and interfaces to other systems (Fig. 2). These break down into 12 smaller components, including three design languages, two interfaces with their corresponding protocols, a schematic versus layout comparison system, and two verification systems—one for simulation and one for timing analysis. Also included are four modules from Genesil—the Genesil data-base-management system, module- and chip-layout synthesis components, package library and editor, and the system that generates the mask and test tapes and the chip plots.

GCX, a proprietary design language that is an extension of C, and a language compiler for it, are part of the Genesis system. GCX is used to create the layout and timing-model synthesis components of a silicon-compilation system. This layout synthesis language understands the application that it is trying to implement and is optimized for creating layout-compilation engines.

Another design language, FCX, and its compiler are used to describe the functional behavior of the circuits created with GCX. This description is subsequently put into the functional simulator analyzer. The third design language and compiler created for Genesis is ICX, which is used for defining human interfaces, such as windows, forms, and various types of menus. Users can create comprehensive human interfaces with a few brief lines of code. ICX also automatically synthesizes schematic diagrams.

Because GCX is an extension of C, it can be used by itself for a variety of other tasks. With GCX, Genesis users can create stand-alone compilers that simply generate layouts. It is powerful enough to not only provide an optimized way of describing technology-independent parameterized layouts—layouts that can be changed for different IC technologies simply by changing a few parameters—but also to define behavioral and functional simulation models, read and interpret technology data bases, or even define human-machine or machine-machine interfaces. For example, GCX could be used to build interfaces to any of the user's existing development systems, simulators, or analysis packages.

But to make life easier for the user, Genesis also contains two built-in interfaces and protocols for reaching out to other systems. One interface enables users to supply physical design data developed on their own design systems in the GDS II format. The protocol includes timing and schematic information for those users who do not have access to schematic work stations. The second interface is designed for those users who have their own schematic work stations and wish to transfer schematic and timing data defined with them to the Genesis system.

Also built into Genesis is a system that compares the results of a layout compiler with the schematic to verify whether the layout compiler is correct. Another comparator does the same thing for simulators by comparing the functional-level simulation to the switch-level simulation. A third verification system, the timing-analysis verification system, generates a complete model to be run in Spice to verify the accuracy and correctness of the timing analysis of the compiler produced using Genesis.

When all 12 parts are connected, the result is Genesis, an overall framework for IC development through silicon compilation. Why this framework is needed can be illustrated with an example. One day an engineer may design a family of RAMs. Then he may design a PLA family. Sometime later, these may be combined on a chip. A smart silicon compiler will need enough global information to make sure that this combination happens correctly. How all the pieces will fit together has to be figured out in advance by the compiler-system builders. At Silicon Compilers, building this framework consumed about 40% of the development effort—$4 million of the $10 million spent by Silicon Compilers in developing Genesis and Genesil—according to Johnson. Another $4 million was spent in building all the verification modules to make sure that what Silicon Compilers built and what users build with it are correct. ☐

HOW A SINGLE-FIBER OPTICAL LINK CARRIES TWO-WAY DATA FLOW

RAYCOM CUTS CONNECTION COSTS BY TAMING REFLECTION

Simultaneous bidirectional communication over a single thin strand of fiber-optic cable pioneered by Raycom Systems promises to greatly reduce the time and expense involved in local-area communications. By combining an easy-to-use connector system with low-cost lightweight cable, the Boulder, Colo., company hopes to snare part of the huge market now held by coaxial and twisted-pair cabling.

The crucial components of Raycom's link are the Y-shaped couplers, which are joined to single-fiber cable. These bifurcated couplers join respectively to a p-i-n diode and a light-emitting diode and terminate in a unique dry-connector system. The connectors mate with the cable in a way that minimizes crosstalk as well as near- and far-end reflections.

Fiber-optic transmission is already replacing copper cable and microwave links in long-haul communications. IBM Corp. and AT&T Co. are touting high-speed fiber local-area networks as the way to link clusters of buildings. But for low-cost, low-duty-cycle applications such as sharing peripherals or linking sensors and controllers in factories, fiber is just taking off [*Electronics,* Sept. 2, 1985, p. 30].

Many of the characteristics that make fiber attractive in long-haul communications make it useful for short-haul as well. Chief among these are blinding transmission speed, large bandwidth, low loss, immunity to electromagnetic and radio-frequency interference, and its inherent security.

But high component costs generally have kept fiber optics from grabbing a chunk of the cost-sensitive short-haul market, though this could change fast if Raycom's single-fiber solution takes off. "A single-fiber-network solution reduces by half the cost of cable and in-line connectors compared with a duplex fiber cable—and any splices or connections needed to reconfigure the network can be made by untrained personnel using a specially designed cable-termination kit," says Raycom's president, Paul Adams.

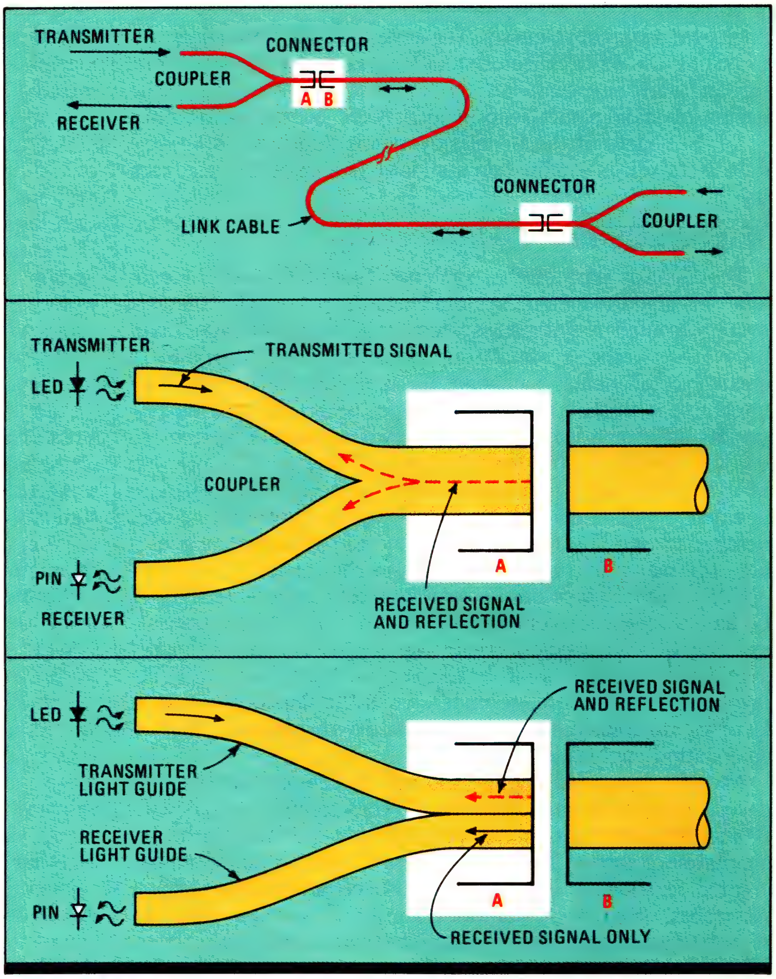
To develop simultaneous bidirectional transmission on a single step-indexed fiber, Raycom succeeded in taming the problem of reflection—the principal source of signal interference on fiber-optic networks. "Reflection was the big impediment in the way of simultaneous bidirectional transmissions," explains Raycom founder and chief scientist Karel J. Kosman. "For all practical purposes, these reflections cannot be eliminated in any link that uses rejoinable connectors."

In a fiber link, each connection point represents a discontinuity. Reflection occurs at each optical surface as light pulses pass from the transmitter cable to the carrier fiber, across any cable splices or node connections on the local link, and into the receiver cable. As the transmitted light passes through the glass-to-air-to-glass transition at the connections, some of it is reflected by the cable end back toward its source. If two transmissions from opposite ends of the link occupy the light guide simultaneously, reflections may be confused with signals at the receiver, producing a read error.

Kosman says the most common solution to this problem is to use wavelength-division multiplexers at either end of a cable. Sending light pulses at two different wavelengths makes it easier to differentiate reflection noise from a true signal. But adding the required costly hardware is an impractical solution in any system that aims to be competitive with coaxial cable or copper twisted pairs.

To come up with a system suitable for a cost-sensitive market, Raycom solved two related problems. Rematable connectors are a must in any short-haul optic link, but the air gap at the mating of the two connectors represents a discontinuity. According to Kosman, other companies have used a connector containing a fluid or gel in the connector to match the optical index of refraction at the gap to effectively eliminate the discontinuity. But the complexity of assembling such a "wet" connector is often difficult for unskilled personnel to master.

Another problem lies in the design of single-fiber optical



1. NO REFLECTIONS. In a single-fiber optical link (top), most reflections occur at the connector (A and B). Couplers that mix transmit and receive signals cause reflections (middle), so Raycom's coupler optically isolates the two paths (bottom).

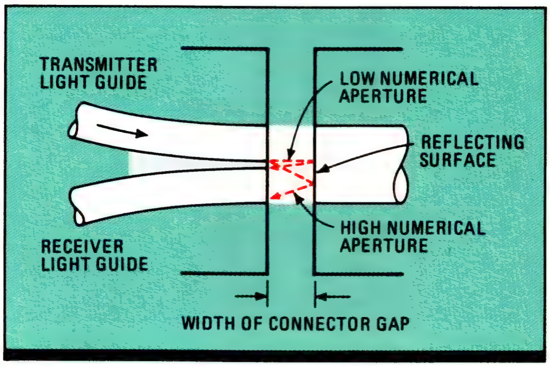
couplers, which split the single optical-fiber link into transmit and receive paths. A section of such couplers evenly distributes the incoming light between the two branches; though this mixing section evenly distributes the desired signal, it also evenly distributes reflected energy. If these reflections are at the same wavelength as the signal, they will make true signal determination impossible.

"We got around these problems by incorporating bidirectional couplers within the dry connectors, thus eliminating any a mixing section between the coupler and connector," explains Kosman. "Reflections still occur, but now the reflected energy can be prevented from overwhelming the incoming signal."

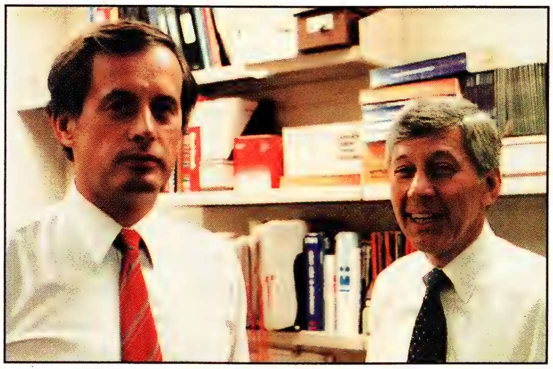
Raycom's solution attacks the three sources of reflections: reflections at the surfaces of mated connectors that are closest to the signal source and far-end reflections from remote connectors. In a simple link (Fig. 1, top), the first surface of the first connector (marked A) is the dominant source of reflection in the link. The second surface of the connector (marked B) and all other connector surfaces are secondary sources of reflection.

In many other designs, the coupler's transmit and receive branches are merged into a single strand before the first surface of the near-end connector. Such a design acts as an integral mixing section, causing reflections to be distributed evenly between transmitter and receiver (Fig. 1, middle).

Raycom's design eliminates such mixing by moving the coupler to the tip of the first connector as well as optically isolating transmit and receive paths (Fig. 1, bottom). This adjustment confines reflection to the transmit branch; thus it cannot mix with the incoming signal on the receive branch.



2. SECOND SURFACE. Optimizing the separation between light guides controls reflection at the second surface.



3. MAIN MEN. Raycom's Kosman (left) and Adams say their system may replace coaxial and twisted-pair cabling.

Controlling reflection at the second surface of the connector requires more care, because it is necessary to control the separation between the two light guides, the numerical aperture (an expression of the degree of divergence of the beam emerging from the light guide, measured as the sine of half the angle of divergence), and the gap between two fiber ends in the connectors (Fig. 2).

Separating the two light guides means that less light will be reflected from the transmitter into the receiver. But a large separation creates a dead area between the two light guides, which lowers the receiving efficiency of the coupler. The loss of efficiency is a function of signal spreading over three surfaces: the receiver, the transmitter light guide, and the dead area. The larger the dead area, the greater the receiver sensitivity must be, but an increase in receiver sensitivity further increases the susceptibility to reflection.

By controlling the numerical aperture of the transmitted light, it is possible to limit the amount of reflection from the second surface of the connector. Low-cost LED transmitters typically emit a fairly wide cone of light, which tends to propagate down the line in lossy higher-order modes.

A typical cable attenuates the higher-order modes faster than the lower-order modes over distances ranging from several feet up to hundreds of feet. In such cases, the higher-order modes are less prominent, so the numerical aperture of the transmitted light is reduced. However, in short cable, the numerical aperture tends to remain high.

The Raycom coupler promotes the attenuation of the high-order modes by mode stripping, a method that involves bending the fiber to accelerate the higher modes out of the light guide and into the cladding. The cladding itself is surrounded with a light-absorbing medium that removes the higher-order modes from the cladding. Raycom will not divulge the composition of the materials, but it claims they remove close to half the total light energy of the high-order modes.

STRIPPING HIGH-ORDER MODES

Stripping the high-order modes in the coupler during the beam's launch eases the problems of light reflected from the second connector surface into the receiver light guide. Stripping also reduces the energy in a short cable length. It does not affect long-cable transmission, however, thus easing the dynamic range requirements to the receiver.

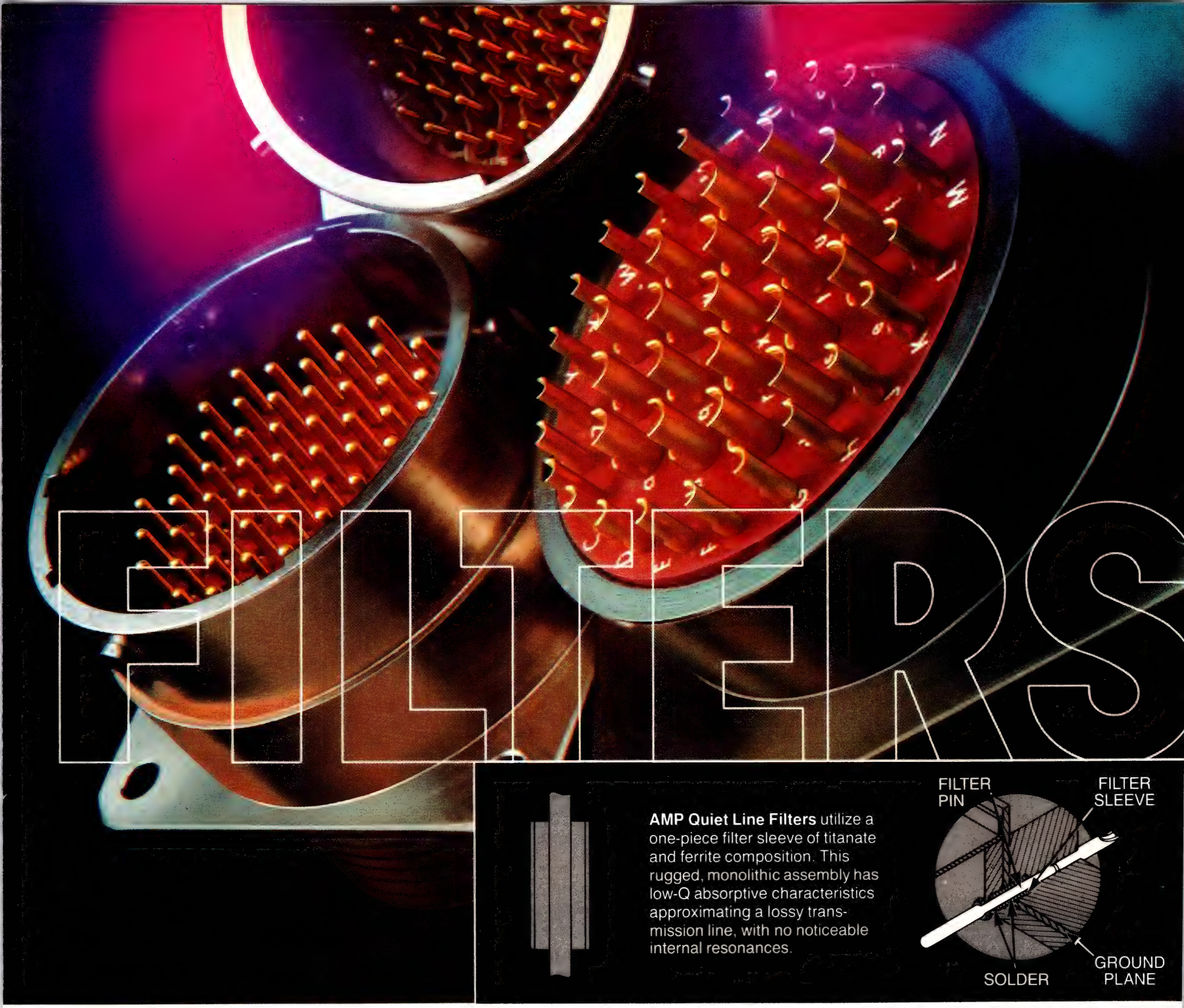
Reflection at the second surface of the connector is also controlled by the width of the air gap separating the two connector faces. A minimum gap is needed to prevent the mechanical interference between optical surfaces during mating; in low-cost connectors the gap is typically around 5 μm or more. But as the connector gap increases, some reflected energy falls back into the receiving light guide and much of the signal energy is dissipated in the dead area, lowering coupling efficiency.

By optimizing the numerical aperture of the transmitted light, Raycom claims to maintain reliable duplex operation with a connector-gap width of 25 $\pm$ 20 μm. The ratio of forward signal energy to the reflected signal is better than 36 dB at the first connector, which is below the sensitivity of most fiber-optic receivers.

To dampen far-end reflections, Raycom designers take advantage of the fact that reflections encounter forward and return loss in the link, while signals encounter forward loss only. A minimum link of 30 ft makes it possible to guarantee an acceptable minimum of the reflection. Raycom also increases reflection diffusion through the link by specifying a slight texture or rough polishing of the cable ends of the link during field termination, rather than a mirror finish.

Raycom's cable diameter is just 3 mm, making a long pull relatively easy. Ensign-Bickford Co., Simsbury, Conn., makes the 200-μm-diameter core and the 230-μm-diameter cladding. Pirelli Cable Corp., Union, N. J., kept the weight of 1,000 ft of cable to around 7 lb while meeting Raycom's tough specifications for flexibility, bending, and tensile strength. Attenuation is below 8 dB/km.

Kosman is betting Raycom's fiber-optic transmission system has a good chance of replacing copper in many short-haul applications (Fig. 3). DuPont Connector Systems, New Cumberland, Pa., took part of the action early this year by signing a joint marketing and development agreement with Raycom. DuPont sees fiber-optic data communications as an emerging market and says that of all the companies pursuing single-fiber simultaneous bidirectional communications, only Raycom has the bugs worked out and an established market position. ☐



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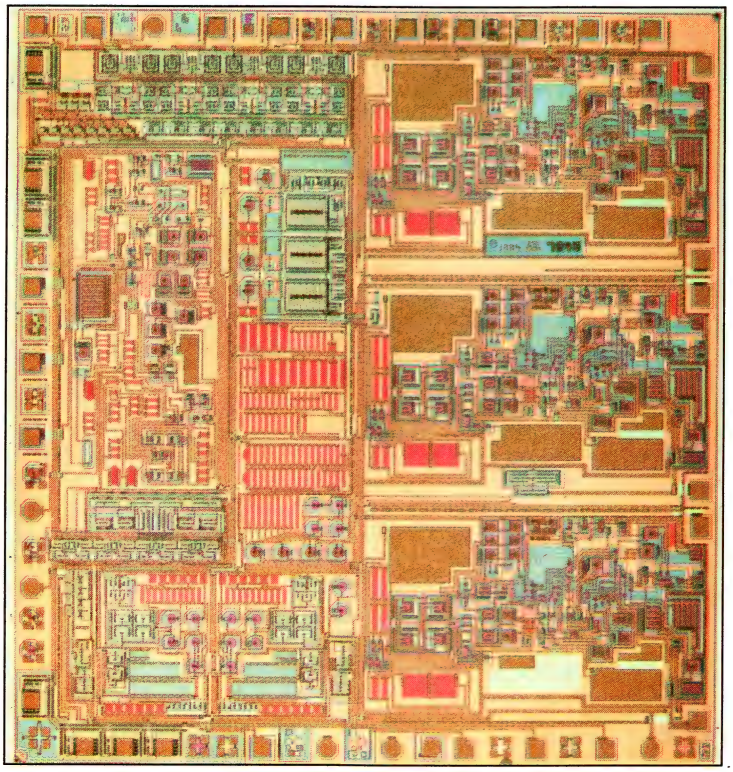
TECHNOLOGY UPDATE

2

SEMICONDUCTORS

THE SURPRISES WILL CONTINUE NEXT YEAR

by Bernard Conrad Cole

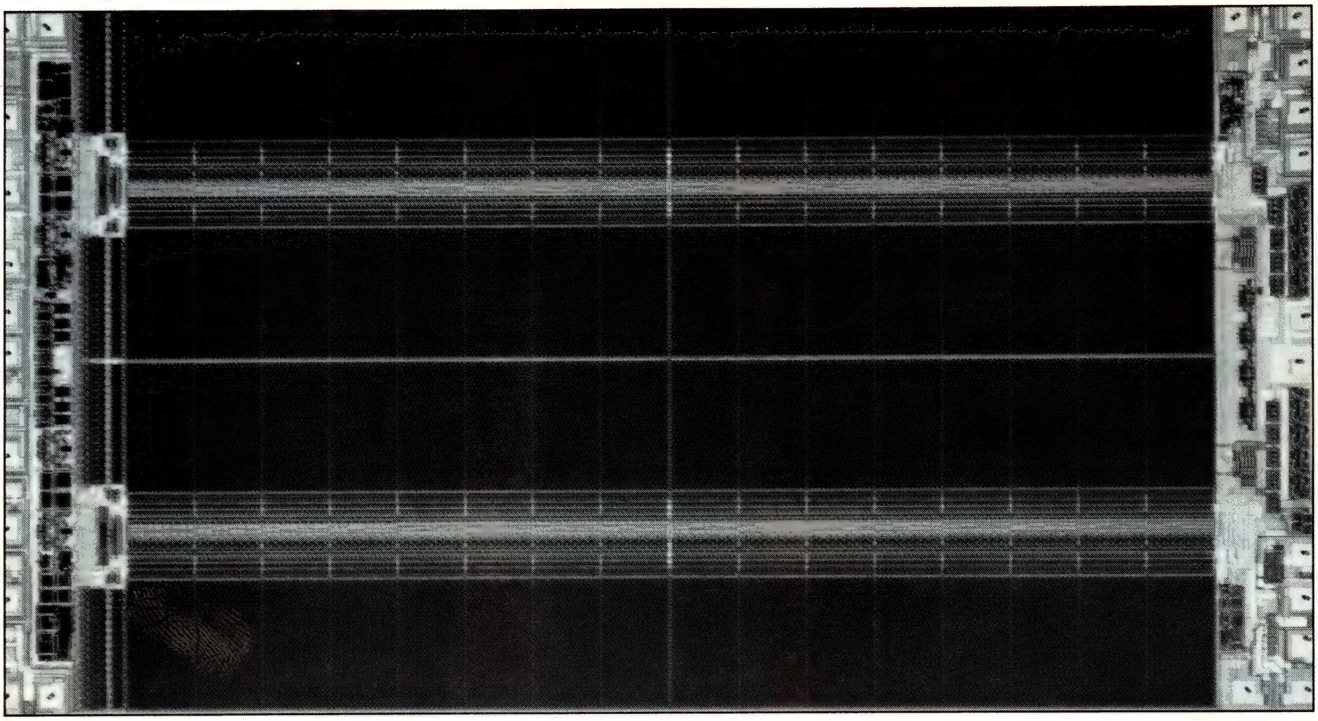


New and revamped processes coupled with innovative circuit designs are bringing about many surprising changes in the capabilities of logic, memory, and linear circuits. While CMOS is sweeping through a major share of chip designs, including linear, bipolar advances are bringing devices that are competitive with MOS in density and power. Part 2 of a 5-part series.

The next 12 months will be stuffed with surprises if semiconductor technology continues to evolve the way that it has during the past year. Some of these changes will be unpleasant and will require a rethinking by the industry of basic processes and methodologies. This is especially true of those used in the design and fabrication of high-density high-performance MOS memory and logic. And in bipolar, emerging static memory and logic devices using techniques developed originally for MOS circuits not only run faster than their MOS counterparts but also compete in density and power dissipation. In linear integrated circuits, designers continue to disprove the commonly held belief that high-performance analog functions cannot be designed with state-of-the-art CMOS processes.

The marketplace is also providing its own surprises, forcing technology changes not foreseen a year ago. In recent months, for example, memory-chip vendors determined that the market for 256-K dynamic random-access memories had fizzled out as far as any significant profits were concerned, so they started pushing harder to develop the next-generation 1-Mb chips [*Electronics,* Sept. 30, 1985, p. 30]. Yet several industry observers believe these vendors are ignoring a number of opposing signs and setting themselves up for a fall.

First, there is the question of acceptance by the customer, who has gotten used to the pace of memory-chip development. "If one looks at the history of RAM development, memories have doubled in size over a period of about every two to four years," says Peter Bagnall, executive vice president of Visic Inc., a San Jose, Calif., memory-chip startup. "Now major memory vendors are looking



HRAM. Visic Inc.'s 64-K hierarchical RAM combines both dynamic and static features, allowing random read, write, and cycle times of 35 ns to any bit in the array. The HRAM's cells are dynamic, but memory is addressed as though it were static.

to skip quickly over the 256-K DRAM and go to the 1-Mb as soon as possible, in direct opposition to institutional and technological momentum and the needs of the marketplace, which is for low-cost and high-reliability memory products."

Second, there are still some basic problems to be solved before megabit DRAMs can be produced in volume, much less at a cost or reliability to match 256-K DRAMs. As a result, "the 256-K DRAM is going to be much stronger and longer lasting than any previous generation of product," Bagnall predicts. "Indeed, the 256-K DRAM will be the major DRAM of choice for the next three to four years."

The 256-K's vitality has more to do with the limitations and problems at the 1-Mb level that have to be solved before the larger chips are accepted in the commodity market. "The 256-K devices now available are in most cases simply extensions of well-known 64-K DRAM technologies with no special tricks and, at 2½ to 2 μm, no real scaling problems," says Bagnall. "At the 1-Mb level, everyone is pushing down below 2 μm toward 1 μm in order to get an eightfold increase in density, requiring entirely new methodologies and process techniques, none of which is that well understood."

Each new technique presents as many problems as it tries to solve, declares Sunlin Chou, director of technology development at Intel Corp.'s Portland, Ore., facility. These techniques include trench-type isolation, storage-capacitor dielectrics, triple polysilicon layers, and low-resistance gates.

ALTERNATIVE STRUCTURES

Signal strength and access time also become troublesome as densities increase. "As interconnect lines within the memories get longer, density increases, capacitances increase, delay times are retarded, and access times slow down," says Bagnall. To overcome this, memory makers have been looking to alternatives to multilevel metal layers, such as silicides and self-aligned silicides (salicides) and, more recently, various refractory-metal methods.

Indeed, the industry has already begun moving from the more resistive, conventional doped-poly-gate interconnection materials to higher-performance refractory metal silicides and salicides, most often in a silicide-poly structure. The move to low-resistance metals will continue to the 1-Mb level, and serious consideration is being given to pure refractory metals such as tungsten and molybdenum. Although pure refractory metals have yet to find their way into high-volume 1-Mb DRAMs, their use in gates can lower gate-level sheet resistance by two orders of magnitude over conventional silicon-gate technology.

Beyond the technical problems of getting 1-Mb DRAMs of sufficient quality and reliability, says Bagnall, there are the problems of manufacturing the devices in sufficient quantity to allow the economy of scale to push costs down. "To be a contender in the commodity-DRAM business, a manufacturer must have a facility capable of turning out about a million units per day, at a minimum," says Bagnall. "At the 256-K level, this requires a dedicated facility that costs as much as $200 million and takes one to two years to bring up to production." And because of the fine lines required for 1-Mb DRAMs and the radically different process technologies, manufacturers are faced with integrating an entirely new generation of fabrication equipment into their production facilities. Getting to volume production of 1-Mb DRAMs will require at least two years of development, he says.

Because of production limitations and the high initial cost of manufacture, DRAM makers are developing architectural alternatives aimed at smaller application-specific-chip markets where the average selling price is higher and the volumes lower, away from the traditional by-1-bit configurations to by-2, by-4, by-6, by-8, by-9, by-12, and even by-16-bit configurations. At the 256-K level, this is already occurring, with the by-4-bit architecture becoming increasingly popular.

APPLICATION-SPECIFIC MEMORIES

Likewise, the demand is growing for application-specific memories, such as video RAMs, which are by-4-bit configurations with special input/output circuitry added. "At the megabit level, this trend will increase," says Bagnall. "Instead of just one or two configurations, we will see a dozen or so different styles of DRAMs specific to certain needs." By the end of 1986, fully half of the 256-K units will be in configurations other than by-1-bit, he says. When 1-Mb DRAMs reach full maturity, about 60% will be in configurations other than by-1-bit, Bagnall predicts.

During the next year, static-RAM manufacturers will be assessing what steps to take to the next level of upward integration. Coming into production are 64-K SRAMs in the 45- to 90-ns range. The few 256-K products beginning to appear have access times in the relatively slow 150- to 200-ns range.

But it will be difficult for SRAM makers to continue along the fast-track access-time curve they have enjoyed and still boost density. Richard Pashley, director of technology development at Intel, Santa Clara, Calif., believes the 256-K level for SRAMs represents a barrier even more daunting than 1 Mb is for DRAMs. "Most of the improvements in speed and density to date have come from replacing the traditional six-transistor SRAM cell with a four-transistor one. Application of scaling and various process improvements such as silicides, salicides, refractory metals, and multilevel interconnects will take us only so far—but not far enough to get to 1 megabyte and still maintain a speed advantage over DRAMs. For that, we will have to wait for some sort of conceptual breakthrough that will allow us to replace the four-transistor cell with something that is even more compact."

And, Bagnall believes, there is no neat and simple way in existing technology, such as trench capacitors or some other method of vertical integration in DRAMs, to achieve higher densities and speed in SRAMs. "In addition to all the problems faced in scaling DRAMs, SRAMs have a set of problems of their own. One of the most critical is the increase in noise levels within chip, making it difficult to read and write at high speeds." Thus, he predicts, the 64-K SRAM will remain the predominant high-speed MOS—at least for a while.

EPROMS REACH FOR 1 Mb

Perhaps the most significant development in the nonvolatile memory market during the next year will be the dominance of the MOS ultraviolet-light-erasable programmable read-only memory, and the retreat of mask-programmable ROMs to a few high-average-selling-price niche markets. Indeed, 1986 may be the year of the 1-Mb EPROM, with at least three or four companies following industry leader Advanced Micro Devices Inc., Sunnyvale, Calif.

Traditionally, ROMs have maintained a price and density

HITACHI'S MAKIMOTO MOVES CMOS INTO THE FAST LANE

by Charles L. Cohen

Work done by Hitachi Ltd.'s Tsugio Makimoto set in motion the semiconductor industry's move to CMOS for high-performance microprocessors, logic, and memories. As project manager of the team that developed the Tokyo company's first Hi-CMOS static random-access memory, he demonstrated that CMOS chips no larger than their n-MOS counterparts could reliably attain n-MOS speeds. And somewhat ironically, his team's work also contributed valuable process technology that ended up in Hitachi's 16-K n-MOS dynamic RAMs, which were developed a short time later.

The informed wisdom of the time said that the Hitachi product could not hope to compete with its formidable n-MOS competitor, Intel Corp.'s 2147, a 55-ns 4-K-by-1-bit SRAM. But Makimoto orchestrated the system design and process development, switched to 3-μm design rules rather than the larger ones then in general use, and used gigohm polysilicon load resistors on top of the memory cells. The result: speed equal to that of the n-MOS competitor, smaller chip size, operating power reduced by 8 to 1, and standby power cut by a factor of 1,000.

But CMOS was still regarded with skepticism. Makimoto recalls that although everybody who sampled the product in 1978 praised it, there were few orders after production started in 1979. Particularly in the U. S., people doubted the reliability of CMOS and wondered if it could be produced.

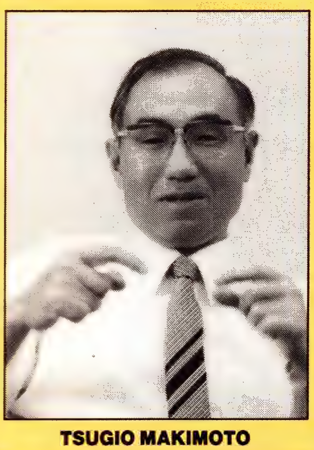
Even though samples were good, customers also backed off because there was no second source. "Fortunately, we believed the praise and kept on producing despite the lack of orders," Makimoto says. "We also developed and produced a 2-K-by-8-bit part that was faster than similar n-MOS and pure-CMOS devices made by others. Customers saw the inventories, compared performance, and were willing to buy both devices."

At the 16-K level, only Hitachi had Hi-CMOS-type SRAMs. But manufacturers applied similar processes at 64-K, and now everybody uses it for 256-K, says Makimoto. He says that Hitachi went to CMOS for the second version of its 256-K DRAM, and all products at the 1-Mb DRAM level and new processor level are CMOS.

Makimoto, 48, is now deputy general manager of the company's Musashi Works, which specializes in MOS devices. In 1959, newly graduated from the University of Tokyo with a degree in engineering physics, he was in the first group of new hires to be employed at the plant.

Only two years of his career have been spent elsewhere. He spent one in the U. S. at Stanford University, studying device modeling with John Linville, and another at Hitachi's Central Research Lab. Timing was fortuitous in both instances. His studies at Stanford came just as course emphasis was switching from silicon transistors to small-scale integrated circuits. The sojourn at the lab came just as the plant was switching from SSI to large-scale integration for use with calculators.

Makimoto treasures the memories of his master's degree studies at Stanford. He recalls that the work pace was especially grueling because the alternative for his fellow students was being shipped to Vietnam.

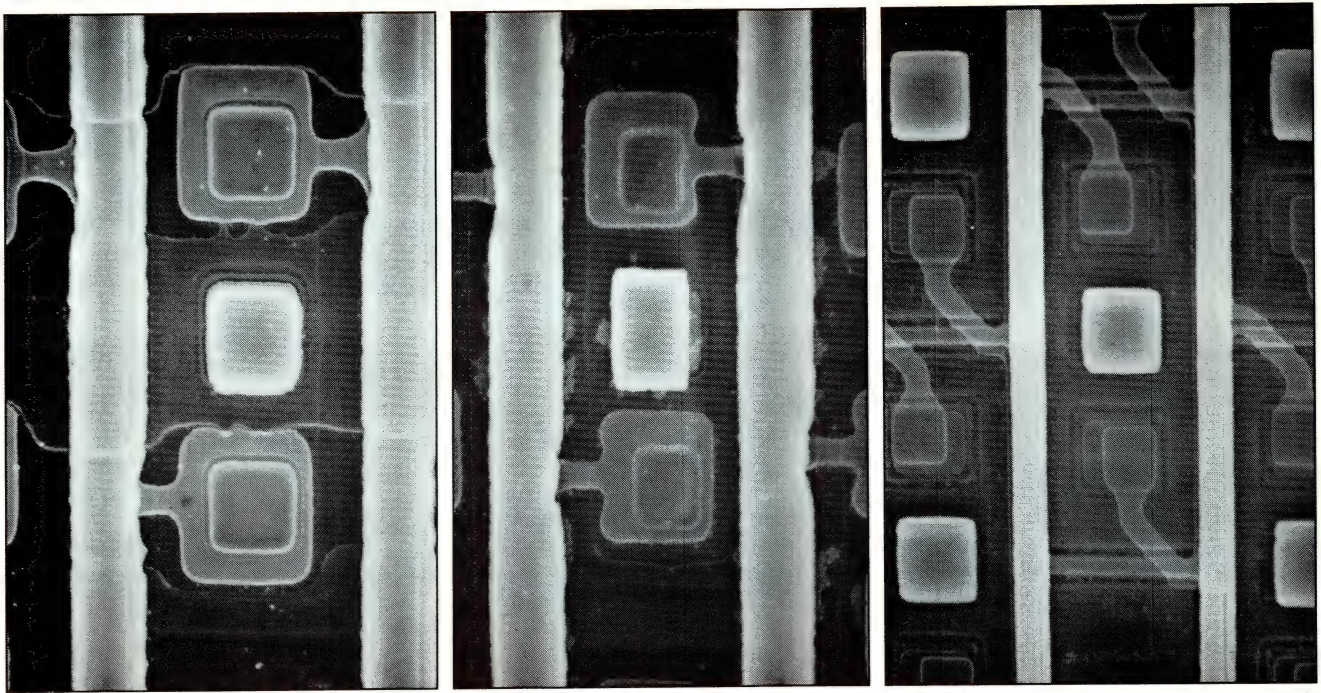


TSUGIO MAKIMOTO

There was a gap between U. S. and Japanese technology at the time. The technology was changing, and it was a golden age at Stanford with professors Linville, Moll, Pritchard, Pearson, and seminars with transistor coinventor and Nobel laureate William Shockley. "Relations between Japan and the U. S. were excellent," he says. "Everybody received me warmly. I am fortunate in having made so many fine friends with whom I am still on the best of terms."

For the future, Makimoto sees the coming decade as the age of application-specific integrated circuits. Because minimizing turnaround time will be a major hurdle, he is particularly bullish on Hitachi's Z-TAT (for zero turnaround time) microprocessors. The plastic-packaged chips incorporate one-time-programmable read-only memory for zero turnaround time. Thus Z-TAT chips can be put on a shelf and programmed to order, eliminating the usual two- to three-month turnaround.

The chips solve most problems of single-chip microcomputers. Development time is shortened by several months, costs are lowered for production runs of several thousand, and maintenance parts are available without storage of inventories of all codes. ☐



IMOX SHRINK. Self-aligned transistor structures using deep-groove isolation take up less cell area than conventional transistors. Feature pitch was reduced from 9 μm in Advanced Micro Devices Inc.'s IMOX II (left) to 7.5 μm in IMOX IIS (middle) to 5 μm in IMOX III-S.

edge on the slightly more complex UV-EPROMs. But with the introduction of 1-Mb EPROMs by such companies as AMD this year, and by companies such as Intel, Motorola, National Semiconductor, and Texas Instruments during 1986, the last nail in the ROM coffin may have been hammered in.

Designated the Am27C1024, AMD's 1-Mb EPROM [*Electronics,* April 22, 1985, p. 52] is fabricated using a 1.5-μm double-poly-gate CMOS process resulting in a die size under 80,000 mils^2. The memory core consists of an array of scaled n-MOS stacked-gate transistor structures, surrounded by CMOS peripheral circuits, with the first poly layer forming the floating gates. The gates are programmed by hot electron injection from the transistor channel region. Organized as 64-K words of 16 bits each, the Am27C1024 features a maximum access time of no more than 170 ns and a programming time of no more than 50 s for the full array. Memory cell size is 20¼ μm^2. With further shrinking of device dimensions, however, cell sizes of 12 μm^2 are possible, allowing at least a fourfold increase in density to 4 Mb.

Not far behind are Intel, with its n-MOS 27513, containing four 16-K-by-8-bit arrays, and NEC, with its MBM27C512, configured as 64-K by 8 bits. At the 256-K level are Tokyo's Hitachi Ltd. and VLSI Technology Inc., San Jose, Calif.

EEPROMs BREAK THROUGH TO 256-K

With the announcement in February of a 100-ns, n-MOS, 256-K EEPROM from Toshiba Corp. [*Electronics,* Feb. 11, 1985, p. 51], many in the industry expect to see a flood of competitive circuits. So far, most manufacturers are standing pat at the 64-K level, waiting for their inventories to drop, prices to increase, and the economy to improve.

First out will probably be Xicor Inc. with its 32-K-by-8-bit X28256, fabricated with the Milpitas, Calif., company's high-performance, thick-oxide, floating-gate n-MOS. It features a 150-ns access time and a 31-μs-per-byte write time, enabling the entire memory to be written in less than a second using a 64-byte page-write technique. Originally scheduled for introduction this summer, it has now slipped to the first quarter of 1986. Intel, which recently signed a technology-exchange agreement with Xicor, is expected to follow soon with its own 256-K n-MOS EEPROM. Xicor is also in development on a CMOS version, the X28C256, with identical access and write times but much lower active and standby power.

While established mainline memory manufacturers slug it out for domination of the commodity DRAM, SRAM, and EPROM business, a new market niche is opening up for application-specific memories. Speeding into this niche are such new startups as Portland's Lattice Semiconductor Corp. and Visic as well as semicustom firms including LSI Logic Corp., Milpitas, and VLSI Technology.

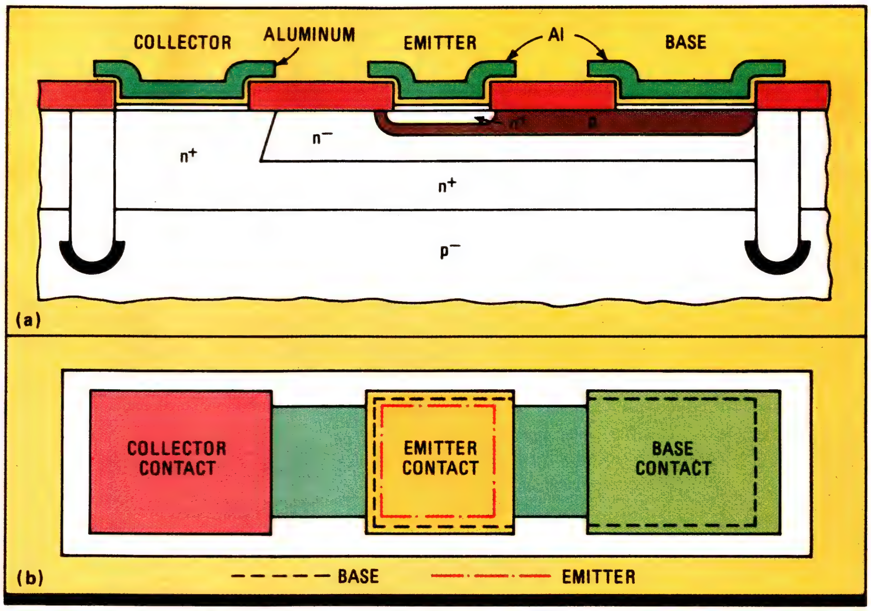
Memory houses have turned to designing their circuits with a variety of operating modes, such as page, nibble, extended nibble, and static-column decode, to increase data throughput and memory-system bandwidth. Visic, on the other hand, has designed an innovative hierarchical RAM (HRAM) that combines both dynamic and static features.

In Visic's first HRAM, a 64-K device, the main memory is a 64-K-by-1-bit array matrix plus two static buffers. Although these cells are dynamic, memory is addressed as though it were static, eliminating some of the complications of DRAM access. Though the dynamic cells must be refreshed, this is accomplished in about 0.1% of the cycle time, versus about 1.6% for standard DRAMs. The architecture allows it to operate in three access modes. In the first, the HRAM allows random read, write, and cycle times of 35 ns to any one of the 64-K bits of information in the array. In a static-column mode, the device can read, write, or cycle to any of 1,024 bits defined by the column addresses in 25 ns. In the third mode, static nibble access and random read accesses to four bits are possible in 10 ns.

In the random-logic arena, semicustom companies are addressing the speed-incompatibility problem of memory and logic by incorporating the memory onto the device. In standard cells, large building blocks of RAM, ROM, and in some cases EPROM are part of the basic cell libraries offered to the customer.

In gate arrays, companies such as LSI Logic offer what are in essence application-specific memories that combine gate arrays and memory. In its LSA2000 series of structured array-logic templates, between 3,000 and 6,000 gates can be combined with 2,300 to 9,200 bits of RAM and 32-K of ROM. The LSA2004, in particular, can be characterized as an applica-

SLOT ISOLATION. Combining isolation slots between transistors with walled emitters dramatically reduces parasitic capacitance in Advanced Micro Devices' IMOX III-S process, permitting drastic size reduction with shorter switching times and base-collector delays.



tion-specific memory, combining 6,000 gates with 9,200 bits of RAM. Built as individual blocks of 2,300 bits each, each block is individually accessible and can be combined to form 26 different architectures using by-4, by-9, by-18, or by-36-bit configurations.

During the next year, the industry could see the first signs of a slowdown in semicustom logic's advance toward higher densities. Both standard-cell and gate-array vendors have had no problem scaling their CMOS processes from 3 to 2 µm, which allowed them to achieve products with densities as high as 25,000 gates (about 100,000 transistors). Further reduction to 1.25- or 1.75-µm geometries could yield densities as high as 50,000 gates for gate arrays and 65,000 for standard cells (about 250,000 transistors). But at such high densities, efficient routing becomes much more difficult, reducing gate utilization considerably—in some cases to as little as 50%.

In standard high-density CMOS logic products, such as advanced 32-bit microprocessors, sophisticated peripherals, digital signal processors, floating-point processors, and some application-specific products for use in such areas as telecommunications, the routing problem is not as acute. This is because, despite a heavy dependence on computer-aided design tools and standard-cell-like techniques, much of the design effort—as much as 50%—is still handcrafted.

A DENSITY BARRIER

Many advanced 32-bit designs to be introduced during the next year call for 250,000-transistor densities, clock speeds in the 12- to 16-MHz range, 1.75- to 2.5-µm geometries, and two layers of metal and one of polysilicon. But unless there is a radical rethinking of the basic process techniques used, the industry will be hard-pressed to proceed beyond 300,000-transistor densities and 25-MHz clock speeds.

As the group most immediately affected, semicustom makers have turned to sophisticated design tools and device topologies with multiple levels of aluminum metal interconnection [*Electronics*, Sept. 23, 1985, p. 48] to keep gate utilization at 85% or better. Many in the industry, such as John Hall, president of Micro Power Systems Inc. of Santa Clara, Calif., believe such hopes are unrealistic because of the industry's current dependence on aluminum and poly as both gate and interconnection material and the use of the self-aligned gate.

The continued vitality of digital bipolar is a big surprise

"The bottom line is that the industry, in applying a number of short-term, low-cost, partial solutions to resolve the serious limitations of the silicon-gate, aluminum-polysilicon approach, has backed itself into a corner," says Hall. The short-term solutions create "a much larger problem, requiring much more wide-sweeping modifications to the basic fabrication process if higher speeds and higher densities are to be achieved."

One of the big surprises of the coming year will be the continued vitality of digital bipolar logic and memory, despite inroads by CMOS and n-MOS. Taking advantage of processing techniques originally developed for use on MOS VLSI chips, digital bipolar technology has advanced steadily to the point where SRAMs can be built as dense as 256-K, with speeds in the subnanosecond range and power-dissipation ratings that are competitive with MOS.

In logic, arrays of about 15,000 to 20,000 gates and gate delays of under 100 ps are emerging. Key process enhancements that account for this improvement are self-aligned device structures, ion implantation, and deep-groove isolation. In memory, much of the improvement comes from the replacement of the traditional resistor-load memory cell with the merged pnp-load cell. Most digital bipolar ICs use relatively conservative design rules, usually in the 1.5- to 2.0-µm range.

Deep-groove isolation, such as that used by AMD in its IMOX III-S slot-isolation process in particular, is a key element in these improvements. Used for isolating the n+ sublayer regions of the bipolar transistors, deep grooves with oxide sidewalls and dielectric fillers (usually undoped poly in the isolation region), provide the needed high breakdown voltage and lower parasitic capacitance while reducing the area occupied by the isolation region. Compared with a conventional transistor with a nonbutted emitter structure, a self-aligned structure using deep-groove isolation requires about one fourth the cell area.

At the high-performance end of the spectrum, digital bipolar technology is proving to be competitive with CMOS in terms of power. Performance of digital bipolar circuits is shielded from serious degradation through the use of 2-V nonthreshold logic, 1.1-V current-mode logic, and 1.0-V merged-transistor logic implementations. Merged-transistor logic circuits, similar to integrated-injection-logic circuits in that they operate in the inverse mode, exhibit circuit delays in the 290-ps range when fabricated using self-aligned transistors. When combined with poly intracell wiring and deep-groove isolation, memory based on merged transistor logic is potentially competitive with CMOS in terms of power, speed, and density. In some 16-K SRAMs implemented with this technique, standby current is in the nanoampere range, equivalent to CMOS memories of comparable size.

One feature of this logic that is exciting some designers is its enhanced resistance to alpha-particle soft errors compared with n-MOS and even CMOS. The key is an n+ sublayer that acts as a common word line, draining away the carriers generated in the substrate by the ionizing alpha radiation and keeping them away from the storage nodes. What is most important about this feature is that it allows the memory cell to be scaled down more than all of the other bipolar alternatives and most of the MOS cells. ☐

IN ANALOG, CMOS IS MAKING THE BIGGEST WAVES

Much of the change now going on in analog-circuit technology comes from CMOS. But the impact will be much less pervasive and more selective than it will in digital circuit technology. "CMOS has its place in analog circuits," says Robert Dobkin, vice president of engineering at Linear Technology Corp., Milpitas, Calif. "But so do bipolar processes, and their dominant position in many areas is not likely to change soon."

Bipolar will be difficult to unseat in several analog design applications. Compared with CMOS, Dobkin says, its strong points are higher voltage gain, more precise matching of critical parameters, lower noise, and higher operating voltages. Linear bipolar also has better dc specifications, particularly higher precision, he adds. For linear functions, CMOS's strong points, Dobkin says, include the ability to fabricate analog switches with excellent characteristics, well-matched capacitors, zener diodes, and the availability of more useful parasitic bipolar transistors. Moreover, MOS transistors generally have very high input impedance combined with very low input currents as well as an input common-mode voltage range that can swing from rail to rail.

CMOS excels in combining analog and digital

Because analog scales down linearly as design-rule minimum dimensions are reduced (rather than scaling down with the square as in digital functions), bipolar also comes out ahead in other designs. Because of this, says Dobkin, bipolar can be expected to maintain its dominant position in classical stand-alone building-block functions, such as operational amplifiers, voltage comparators, and voltage regulators, moving toward higher speeds and greater power-handling capabilities.

Linear CMOS will find its greatest application in those areas where it is necessary to combine both analog and digital elements on one chip, such as data conversion, and in such applications as telecommunications, where whole systems reside on a single chip. Linear CMOS initially will be used in a number of signal-processing applications that until recently have been performed using digital techniques. "One reason many signal-processing functions have gone digital is the belief by many companies that it is not possible to achieve the densities required without giving up on performance," says Chris Stacey, manager of the telecommunications applications group at National Semiconductor Corp. The argument is that the current device geometries, in the 3-to-4-μm range, are unlikely to result in an economical device. "This is far from the case," he claims. National, for example, is in full-scale production with a 2-μm double-metal CMOS process, and in limited production with denser processes in the 1.5-μm range.

Linear CMOS has an additional advantage, he says, in that it generally results in smaller die area per function than an equivalent digital processor. This is particularly true for nonadaptive filtering functions, where an analog design typically has half the die size and half the power consumption of an all-digital design. "Experience is proving that the tighter control of feature definition and the thinner oxides make possible analog performance superior to that achievable on 3- to 5-μm processes," Stacey says. "Specifically, switched capacitor filters have been designed with considerably lower noise than with previous processes."

Making use of linear CMOS's high density compared with bipolar are a variety of semicustom offerings. Most standard-cell vendors, such as VLSI Technology, Gould/AMI, NCR, and Zymos, for example, offer various linear and analog functions as part of their library of standard-cell and megacell functions. In addition, there are a number of analog semicustom offerings available, both bipolar and CMOS.

Linear Technology Inc., Burlington, Ont., has developed a new series of Modula linear arrays that organizes linear components into an array of building blocks. Each block contains varying mixes of standard and Schottky clamped-npn transis-

JOHN HALL WAS CMOS PIONEER WHEN TTL WAS KING

by Denise Caruso

Back in the dark ages of 1970, while semiconductor manufacturers were enamored of TTL, John H. Hall was establishing a new CMOS process for Seiko Co. in Japan. It yielded the world's first large-scale-integration CMOS chip, far ahead of its time as the 1-V heart of the world's first successful electronic watch.

It was also the last aluminum-gate CMOS chip Hall ever designed. "We needed a higher-density technology and realized that silicon gate was not applicable to CMOS," recalls Hall, founder, president, and chief executive officer of Micro Power Systems Inc., Santa Clara, Calif. "So in exchange for me providing assistance to Seiko for building the watch, it provided the seed capital for Micro Power, where we started the molybdenum-gate CMOS process."

Moly-gate CMOS uses thinner layers of material than silicon gate; more separate and distinct layers of on-chip wiring make integrated circuits run faster at lower cost.

But Hall says pioneering the technology had one drawback. No one listened to him. "We tried to tell the press about moly-gate CMOS for years. No one wanted to hear it. They were all too interested in the latest fad—which at the time was TTL."

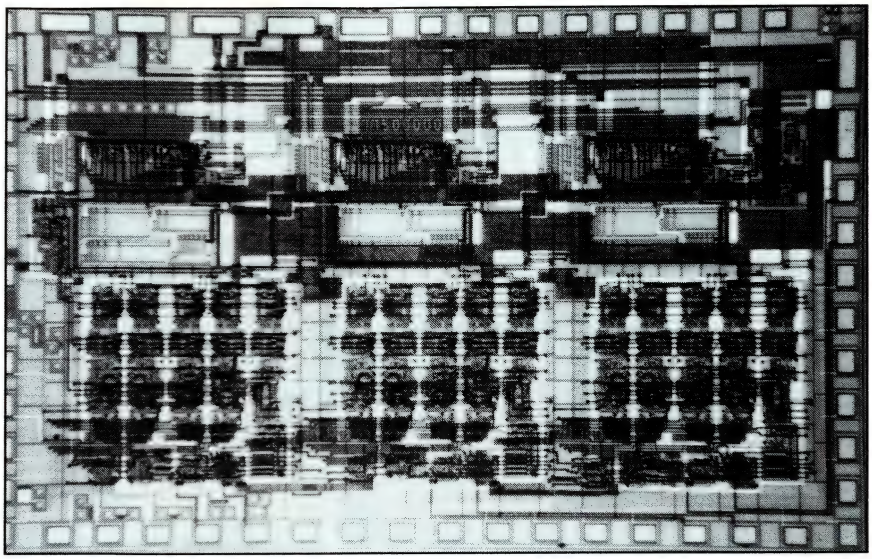
Other firsts in Hall's career include the electronic camera shutter, multiprogrammable heart pacemaker, and the first radiation-resistant IC.

He also founded the semiconductor division of Union Carbide Corp. with Jean Hoerni—also a founder of the famed Fairchild Camera & Instrument Corp.'s semiconductor division—in 1962. But Intersil Inc., a custom IC company also founded by Hall and Hoerni in 1967, was home of the low-power watch circuit whose shortcomings led to the development of moly-gate. "Intersil first got Swiss money to develop a watch IC," says Hall, "We developed a bipolar chip for them, then the Swiss decided not to build the watch."

JOHN H. HALL

Then Seiko was interested, recalls Hall, "but they wanted CMOS. So we had to create the technology—it took us about six months." Initially used in the world's first liquid-crystal-display watch circuit, moly-gate chips are now found in such sophisticated applications as phased-array radar.

Other developments, says Hall, are soon to come. But this time he isn't worried about who listens to him. "The Japanese are already interested in what we are doing now," he says. "They're looking at the next 20 years of technology, not fads."



TRIPLE PLAY. Honeywell Inc.'s DAC34010 and DAC34020 digital-to-analog converters comprise three 4-bit DACs together with logic translation, decoding, and voltage-reference circuitry. The chips can convert 100 or 200 million words a second, respectively.

tors, double-collector lateral pnp transistors, multiple-collector pnp transistors, and based diffused resistors of various values, as well as large npn transistors, low-noise npn transistors, zener diodes, junction capacitors, and pinch resistors on the periphery. Also offered is a library of predefined linear subcircuits, including op amps, comparators, video amps, timers, balanced modulators, bandgap references, and voltage-controlled oscillators.

From Micro Linear Corp., San Jose, Calif., comes a linear array fabricated with a high-density, 12-V, 1-GHz bipolar process that includes ion-implanted resistors and capacitors. The array makes use of what the company calls a linear mosaic, in which an identical grouping of devices, called a tile, is repeated regularly on the chip. Within each tile are npn and pnp transistors of various configurations, resistors, and a capacitor. Also offered is a macrocell library that includes such linear building blocks as linear output buffers, transconductance op amps, video amps, a modem, and comparators.

At International Microelectronic Products Inc., San Jose, a 3-μm CMOS standard-cell approach makes use of two types of analog cells. One consists of basic analog blocks with predefined electrical and topological characteristics, such as op amps, voltage reference circuits, comparators, and so on; the other consists of variable-value elements, such as resistors and capacitors, whose properties can be adjusted for different design environments. The unique feature of this approach is the interconnection strategy, which incorporates separate analog and digital connection channels between rows.

Linear CMOS dominates the data-conversion market, but bipolar technology retains a strong foothold in the high-speed arena. At Honeywell Inc., for example, designers have developed two triple digital-to-analog converter chips, the DAC34010 and DAC34020, capable of conversion rates of 100 million and 200 million words a second, respectively (Fig. 4). Fabricated using an advanced VLSI bipolar process, both chips incorporate three 4-bit DACs, logic for translating TTL and ECL to current-mode-logic, decoding logic, and a voltage reference.

Building blocks for high currents, voltages will keep bipolar ahead

The chips are designed for such applications as video color displays, where a 2,000-line screen may typically have 2,048 by 1,280 pixels refreshed at a rate of 60 to 80 Hz. Each converter is specified for a differential linearity of ⅛ least significant bit and a matching accuracy of 1 LSB. The three converters share a single bandgap reference to ensure close matching, and crosstalk is eliminated by supplying each internal converter with its own reference buffer. Capable of accommodating TTL signals, these input buffers use a nonsaturated input translator to increase speed in excess of that of standard saturated-TTL buffers.

Also designed for video applications is a 12-bit TTL- and ECL-compatible current-mode-logic bipolar DAC chip that can deliver 20-MHz signals, from TRW's LSI Products Division in La Jolla, Calif. Designated the TDC1012, the DAC is designed as a current switching device, so its complementary outputs can drive either transmission lines or external amplifiers.

Linear Technology's Dobkin believes a new target of opportunity for bipolar linear is the design of standard building blocks that can handle extremely high currents and voltages. One example of this trend is a 150-W op amp designed by Mineo Yamatake of National Semiconductor Corp. and consultant Robert Widlar. The op amp has a continuous dc power dissipation of 90 W and a peak power rating of 900 W.

The chip consists of a large array of modified Darlington transistors with emitters joined to the underlying metal through deposited polycrystalline silicon resistors. To maximize emitter area and reduce lateral distance to the collector sinker diffusion, base contacts are made small, more than offsetting the increase in base spreading resistance.

MIXING CMOS AND BIPOLAR

Forever hopeful, analog manufacturers are continuing to look for ways to combine the advantages of both bipolar and CMOS without the disadvantages of both. However, this has gone beyond simply taking advantage of the parasitic bipolar structures inherent in the CMOS process.

Analog Devices, Wilmington, Mass., has developed BiMOS II for its line of high-performance data converters. BiMOS II merges a junction-isolated buried layer on epi process with aluminum-gate CMOS and thin-film resistors. This allows fabrication of vertical npn and pnp transistors, as well as bipolar FETs, on the same device as p- and n-channel transistors.

Texas Instruments Inc., Dallas, uses the BidFet process, which combines double-diffused MOS (DMOS), n- and p-MOS, and npn transistors on the same chip. For use in high-voltage applications, BidFet can fabricate devices with working voltages to 225 V (open drain), 130 V (totem pole), and breakdown voltages exceeding 450 V.

Motorola Inc. uses a third method. The Phoenix, Ariz., company combines metal-gate CMOS and vertical pnp transistors in the design of a variety of op amps and voltage regulators.

One of the most sophisticated mixed processes is that of Micro Power Systems Inc. The Santa Clara, Calif., company combines scalable molybdenum-gate CMOS with a double-diffused buried-layer bipolar process. This method provides both vertical and lateral pnp transistors with betas of 200 and 50, respectively, and vertial npns with buried layers. Micropower's Hall claims the company's molybdenum-gate process allows completely separate interconnection for both bipolar and CMOS devices, unlike silicon gate. Moreover, the buried layer, he says, also makes possible buried zener references.☐

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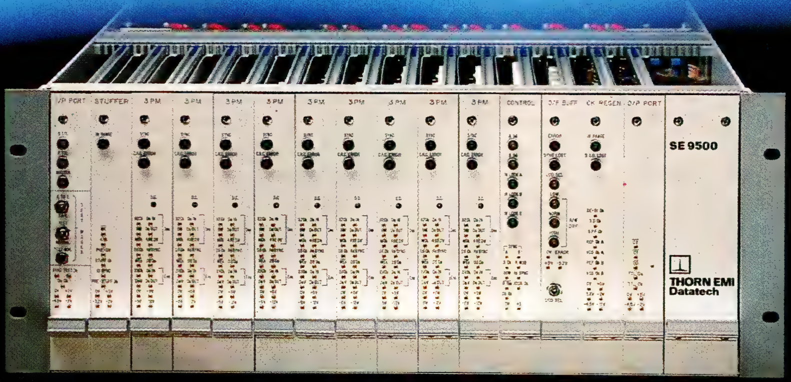

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PRODUCTS NEWSLETTER

AMD RELAUNCHES FUSE-PROGRAMMABLE MICROCONTROLLER

Advanced Micro Devices Inc. is once again announcing the 20-MHz Am29PL141 microcontroller, which it introduced initially 15 months ago [*ElectronicsWeek,* July 30, 1984, p. 58]. Errors in the metal layer of the bipolar fuse-programmable part forced the Sunnyvale, Calif., company to postpone delivering samples, which had been slated for September 1984. The chip is being reintroduced at a much lower price—$32.50 each in 100-piece orders, compared with the original $95. Customers can program the single-chip microcontroller with microinstructions similar to those used on AMD's programmable logic arrays. Deliveries will be made 10 weeks after ordering. ☐

LATTICE SEMICONDUCTOR DELIVERS FAST MILITARY 64-K SRAMs

Lattice Semiconductor is set to take on such heavyweight military-memory suppliers as Harris Corp. and RCA Corp. with a 64-K CMOS static RAM that it is ready to deliver. The SR64K4-45M has a 45-ns access time over the full −55°C to +125°C military temperature range, compared with the 150-ns speed of RCA's 64-K part. The chip is the Portland, Ore., company's first offering in a three-phase program directed toward full qualification to MIL-STD-883C, which is expected to come in the first quarter of next year. ☐

2½-DIMENSIONAL DISPLAY CUTS CAD SYSTEM'S COST

Engineers who want to see objects in perspective but who don't want to spend big bucks to do it can turn to Adra Systems Inc. The Lowell, Mass., firm's Adra-1000 computer-aided-design system provides a 2½-dimensional display with response times under ¼ s. Unlike 3-d solid modeling, 2½-d lets users project two views of an object on a screen to give an isometric-like perspective. According to Adra, this process requires less expensive computers and less technical expertise to program. Priced at $15,570, the Adra-1000 consists of a Motorola 68010-based central processor, 2½ megabytes of memory, a bit-slice graphics processor, and a 19-in. display. ☐

GOULD THROWS ITS WEIGHT BEHIND THE MAP PROTOCOL

Gould Inc.'s Industrial Automation Division, already a familiar name in the factory, is adding its considerable influence in support of the emerging Manufacturing Automation Protocol (MAP). Two products that the Andover, Mass., division is now delivering connect incompatible local-area networks and integrate industrial-automation systems. The MAP Gateway and enhanced Concept Series 6050 computer allow communication among computers made by a variety of vendors; the network boasts a 10-Mb/s data rate. These products implement open-systems-interconnection standards and permit upgrading of current systems without replacing equipment. Both use a 68010-based central processor and run the MTOS real-time operating system. ☐

CONNECTIONS TO 115-kb/s NETWORK COST ONLY $110 PER NODE

Users of personal computers will be able to link their systems, printers, and modems in a network at a cost of about $110 per node with Matrix Communications' Alliance intelligent cluster controller. Currently, network connections average $650 per node. To be unveiled at Comdex in Las Vegas next month, the Alliance links up to 20 pieces of equipment over RS-232-C interfaces operating at 115 kb/s. An optional 480-K-byte buffer is available for print spooling and electronic mail. When the Marblehead, Mass., company delivers Alliance in January, the basic 8-port unit will sell for $895; a 4-port expansion controller will go for $349. ☐

FIRST CELL LIBRARY DEVELOPED FOR CURRENT-MODE LOGIC

VTC's STANDARD CELLS GO UP AGAINST ECL-GATE ARRAYS

Until now, users of application-specific ICs who needed bipolar speed had to settle for gate arrays. But this week, VTC Inc. will release the initial 66 standard cells in its new VL2000 line, billed as the industry's first digital bipolar standard-cell library for designing with current-mode logic. An additional 13 cells will be released in November.

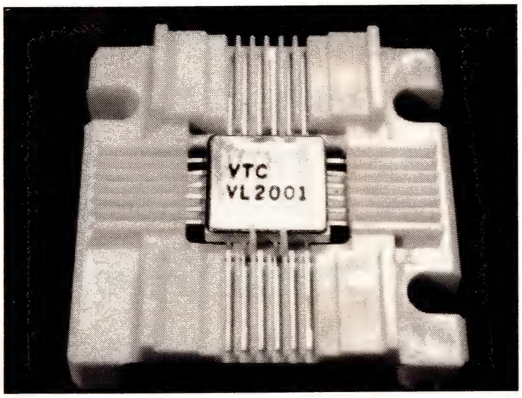
Built in a 2-μm oxide-isolated current-mode-logic process, the VL2000 High-Performance Bipolar Digital Cell Library features typical gate delays of 440 ps or 800 ps, depending on which of two speed-power options is used. I/O buffers are available for compatibility with either TTL or 10KH emitter-coupled logic.

VTC marketing manager George Sanders says the VL2000 line will match up well against bipolar gate-array offerings from vendors such as Advanced Micro Devices Inc. and Motorola Inc. The relatively low power requirements of VTC's current-mode-logic process will provide a superior speed-power product than more power-hungry ECL gate arrays, he says.

Compared with current-mode-logic gate arrays offered by companies such as Honeywell Inc., the VL2000 loses its inherent speed-power advantage. But VTC officials point out that their standard-cell line will provide more efficient silicon utilization and better I/O flexibility than is possible with a gate array. For equivalent processes and the same number of gates, a design based on a cell library typically consumes 25% less real estate than a gate array. What's more, "If a guy needs 100 inputs but only 10 outputs, a gate array won't give him that flexibility," Sanders says. "But with the VL2000, it's no problem."

DUAL-PORT RAM. The library will contain 79 cells ranging in size from a simple OR/NOR gate to an AMD 2901-compatible 4-bit arithmetic logic unit, the largest cell in the library at 150 gates. Along with a range of counters, multiplexers, comparators, and adders, the library will include a 16-by-4-bit dual-port RAM cell. The average VL2000 cell size is in the 25-to-50-gate range, says Gary L. Lutz, product line manager.

VTC specifies power dissipation for two sizes of circuits, based on the assumption that one third of the cells will be using the high-speed options (440-ps gate delays), while the other two thirds will use the lower-power option (800-ps gate delays). In this case, inputs and outputs would be evenly split. Under those conditions, a 1,000-gate 40-pin VL2000 circuit would dissipate 1 W typically; a 4,000-gate device would dissipate 3 W, according to the company.



READY. VTC Inc. now has the first standard-cell library implemented in current-mode-logic technology.

Engineers with access to engineering work stations running software from either Metheus Corp. or Mentor Graphics Corp. can go right to work on designing VL2000 circuits. "All they've got to do is get a copy of our design system [priced at $250] and load up our cells," says Lutz. Personal computer design options are also available using the Metheus software, and VL2000 designs can be simulated on a variety of mainframe computers using the HiLo simulation package supplied by GenRad Inc.

Once design and simulation are complete, customers may deliver a net list to VTC, and the company will transform this list into silicon for an engineering charge of between $20,000 and $40,000. That price includes the delivery to the customer of 15 working prototypes within 10 weeks after delivery of the net list. VTC is prepared to move into production on a part within 8 to 10 weeks after the customer accepts the prototype.

Device pricing will vary according to complexity and package type selected. VL2000 circuits are offered in eight package options. In volumes of 50,000 devices or more, VTC officials estimate prices at around $10 each for a relatively simple design in a 40-pin plastic DIP to more than $100 apiece for a 5,000-gate design housed in a 172-pin pin-grid-array package.

VL2000 devices will be offered for either commercial or military temperature ranges. Though the current-mode-logic process offers good inherent radiation resistance, radiation-hardness tests have not yet been completed; therefore, that parameter will not be specified initially. VTC officials note, however, that preliminary data taken using a simple ring oscillator reveals no performance degradation at radiation levels of 1 megarad.

VTC expects the VL2000 library to find applications in new very large-scale IC designs and in sockets to replace 10KH ECL and TTL devices. Areas of application will include computer mainframes, computer peripherals, and digital signal processing for both military and commercial designs, according to the company. *–Wesley R. Iversen*

VTC Inc., 2800 E. Old Shakopee Rd., Minneapolis, Minn. 55420. Phone (800) 352-6789; or in Minn. (612) 853-4342. [Circle reader service number 338]

TI ADDS CONTROLLER AND RAMs TO VIDEO-CHIP LINE

Computer-graphics engineers have six new video-system components to draw on when they design high-resolution color work stations, personal computers, bit-mapped display terminals, and fast laser printers. Texas Instruments Inc. this week is introducing a single-chip video-system controller and five new packaging options for its 10-month-old TMS4161 64-K multiport video RAM, including chip carriers and single in-line packages.

The new products can reduce the size—and likewise, the cost—of high-resolution graphics subsystems. The 68-pin TMS34061 video-system controller combines all of the circuitry required to control VRAMs, standard dynamic RAMs, and cathode-ray tubes in a single n-MOS IC.

Integrating these control functions eliminates the need for separate text and graphics subsystems, says Ahmed Nawaz, marketing manager for graphics products. "During TI's interaction with customers over the past six months, we have found that the controller will eliminate duplicated functions in text and graphics subsystems, replacing anywhere from 25 to 35 chips," he says. The 34061, available only in a plastic leaded chip carrier, sells for $35.50 each in 100-piece lots.

TI is now offering a 64-K VRAM with a 150-ns access time in a 22-pin plastic leaded chip-carrier measuring 0.290 by 0.490 in. The J-leaded TMS4161FML VRAM will reduce board-size requirements by half compared with DIPs. The surface-mountable VRAM sells for $3.20 each in orders of 100 pieces.

For the single in-line packages, TI is mounting four to five chip-carrier-housed VRAMs on an epoxy pc-board substrate. The SIPs pack about 3½ times the density on a pc board compared to DIPs. A 30-pad leadless SIP that can mount in a socket—the TM4161GW4 64-K-by-4-bit module—sells for $24 each in 100-piece lots. The part has a 150-ns maximum access time. Other package options include a 30-pin leaded SIP, a 31-lead 64-K-by-4-bit SIP, and a 35-lead 64-K-by-5-bit SIP.

The new video-system controller offers programmable control of screen resolutions from 256 by 256 to 4,096 by 4,096 pixels. The unit effectively has the power to double the processing power of host microprocessors (8-, 16-, or 32-bit chips) by taking over 95% of the overhead functions required in high-resolution bit-mapped graphics. It has been designed to provide control of the multiport VRAMs, which have graphics-oriented shift registers that can support dot rates of 5 MHz to beyond 150 MHz.

The 34061 controller has a built-in X-Y addressing register, which acts as a hardware accelerator for the incremental drawing algorithms common in graphics routines. *–J. Robert Lineback*

Texas Instruments Inc., (SC-510), P. O. Box 809066, Dallas, Texas 75380.
Phone (800) 232-3200 [Circle 340]

NEW ROUTER LAYS OUT PC BOARDS TWICE AS FAST

The performance of computer-aided-design equipment for laying out pc boards rests on how fast—and efficiently—the equipment automatically routes pc-board connections. To be more competitive in this area, Calay Systems has added a model with beefed-up automatic routing abilities to its CAD line.

Increased operating speed and an interactive, higher-resolution graphics processor are two of the improvements that mark the turnkey VO4, to be introduced this week at the Automated Design and Engineering Conference in Boston. The VO4 gets its computer power from a Digital Equipment Corp. LSI-11/73, rather than the PDP-11/23 employed by the earlier VO3.

TWOFOLD. In its latest CAD system, Calay has doubled the speed of its automatic routing.

The Calay routers, both old and new, achieve 100% automatic layout using the iterative process—continually repeating and redrawing pc-board connections (or traces) to make room for additional traces. Similar to what a designer does in manually laying out a board, the process is sometimes called rip-up routing.

But the VO4, with the addition of a hardware accelerator and new software routines, performs a comparable routing task about two times faster than the VO3. "Our research and development continues to focus on what makes [the system] most unique, the automatic pc-board router. It is the heart of our system and we are committed to developing it, as we did from the start," says Wolfgang Schenke, Calay's vice president for new product development.

The new graphics processor enables the user to manipulate displays with 2,048 by 2,048 pixels—which is four times the image detail of the 1,024-by-1,024-pixel configuration offered by the VO3.

For better routing and component placement of surface-mounted devices, new software provides additional interactive design tools: user-selectable colors let designers easily distinguish which surface-mounted devices are assigned to what side of the board. Designers can designate oblong pads for land areas, along with the exact location on the pad where the router connects the trace. And automatic scaling handles mixed formats such as 0.040- and 0.050-in. centerline land areas.

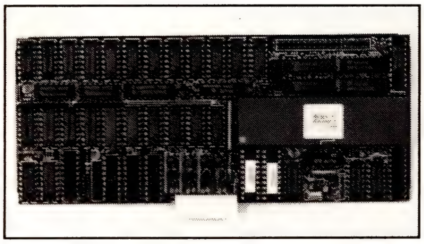
Other major improvements in the VO4 are the hardware pan and zoom features, enabling the designer to quickly scan or view portions of the board.

Available now, the two-station configuration of the Calay VO4 sells for $180,000, LSI-11/73 included. Present users of the VO3 unit may upgrade to the VO4 level with options ranging from $20,000 to $60,000. *–Larry Waller*

Calay System Inc., 2698 White Rd., Irvine, Calif. 92714.
Phone (714) 863-1700 [Circle 339]

iSBX BOARD HOLDS FAST GRAPHICS CARD

The MSBX-900 graphics board, contained on an iSBX card, uses a very large-scale integrated drawing processor that executes more than 35 high-level graphics instructions. With a drawing speed of over 35,000 vectors/s, the MSBX-900 generates displays in less



than 1/3 second. The board, which has a direct-memory-access transfer speed of up to 650,000 pixels/s, can display a Landsat photo in under ½ second.

Display resolution is 640 by 480 pixels, and the board offers 256 colors from a palette of 262,144. The noninterlaced refresh rate is 60 Hz. It performs zoom, pan, and scroll and offers the basic graphics primitives. The MSBX-900 piggybacks onto any CPU board equipped with iSBX expansion connectors, and carries out all communications over the iSBX bus. In single quantities, the units sell for $1,495. Discounts are offered to original-equipment manufacturers. Delivery takes eight weeks.

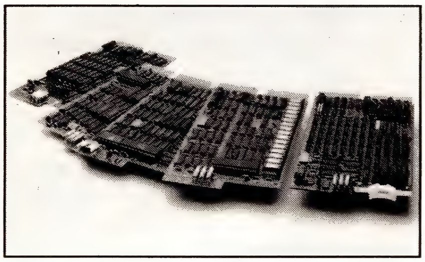
Matrox Electronic Systems Ltd., 1055 St. Regis Blvd., Dorval, Quebec H9P 2T4.
Phone (514) 685-2630 [Circle 364]

GRAPHICS CARDS FIT MICROVAX II

Ten different Q-bus color and monochrome graphics cards plug into the MicroVax II, creating engineering work stations and process-control or medical-imaging systems. At the high end, a $2,995 card offers 256 simultaneously displayable colors from a palette of 16 million with a resolution of 512 by 512 pixels. For the same price, a monochrome card produces dot graphics plus an alphanumeric overlay with a resolution of 1,024 by 1,024 pixels.

Other cards in the series put alphanumeric characters on screen at RAM speeds and add color and character graphics to the on-screen display. All are dual-height cards, and one MicroVax chassis can hold several cards to serve multiple displays. Some cards can be combined. The series sells for $615 to $2,995, and delivery takes 30 to 45 days after ordering.

Peritek Corp., 5550 Redwood Rd., Oakland, Calif. 94619.
Phone (415) 531-6500 [Circle 365]



IBM PC COMPATIBLE COSTS UNDER $1,000

Epson is offering the Equity I, a 16-bit computer compatible with the IBM Corp. Personal Computer, for just $995. The system features three full-size IBM-standard option slots, an 8087 arithmetic-coprocessor socket, a speaker, and front-panel ac-power-reset and option switches. The base configuration includes an 8088 microprocessor, 256-K bytes of RAM (expandable to 640-K bytes), a floppy-disk drive, a built-in Centronics parallel-printer port, and an RS-232-C serial port plus MS-DOS operating system and the GW-Basic language.

Equity I comes in two expanded data-storage configurations—with dual floppy-disk drives, for $1,295, and with one floppy-disk drive plus a hard disk, for $2,195. Delivery starts in November.

Epson America Inc., 2780 Lomita Blvd., Torrance, Calif. 90505.
Phone (213) 539-9140 [Circle 377]

HONEYWELL EXPANDS ITS DSA NETWORK

Honeywell is supplying three processors, the Datanet 8/10, 8/20, and 8/30, for use with its Distributed Systems Architecture (DSA) network. The Datanet machines can serve as front-end processors, switches, concentrators, or any combination of the three.

The Datanet 8/10 supports 31 data communications lines and sells for $23,900. The models 8/20 and 8/30 support 127 and 255 lines and sell for $38,000 and $80,000, respectively.

In addition to the Datanet products, Honeywell is adding a DSA/SNA gateway that users of its DPS 6 computers can use to link with IBM mainframes in a Systems Network Architecture and with other Honeywell computers that follow the open-systems interconnection reference model. Another new product, the DSA6, is the platform supporting the DSA/SNA gateway, along with two-level transaction processng, electronic mail, and terminal emulation.

DSA6 bundled initial and annual primary license fees start at $2,190 and $1,000 each, respectively. DSA/SNA gateway license fees depend on the power range of the DPS 6 system involved.

Honeywell Inc., P. O. Box 8000/A-79, Phoenix, Ariz. 85066.
Phone (602) 862-6140 [Circle 376]

APPLIED DIGITAL DATA ADDS TWO COMPUTERS

The latest computers from Applied Digital Data Systems can be used as stand-alone multiuser systems or linked with the company's larger systems, exchanging data files as needed. The Mentor 1720, for up to three users, and Mentor 1740, for up to eight users, can be expanded by adding terminals, printers, or communication links.

The Mentor operating system under which the machines run is an enhanced, data-base-oriented version of the Pick operating system.

The Mentor 1720 has a 20-megabyte disk and three RS-232-C serial interface ports; the 1740 has a 40-megabyte disk, eight RS-232-C ports, and a 45/60-megabyte ¼-in. tape. The 1720 sells for $7,500 and the 1740 for $12,750, both excluding the Mentor operating system software.

Applied Digital Data Systems, 100 Marcus Blvd., Hauppauge, N. Y. 11788.
Phone (516) 231-5400 [Circle 375]

SPERRY'S PC/IT RUNS XENIX SYSTEM V

With its Xenix System V option, the Sperry PC/IT personal computer can support up to nine users as well as operate as a stand-alone machine. The PC/IT supports the MS-DOS operating system and can house both 8- and 16-bit-based plug-in peripheral cards. The micro-

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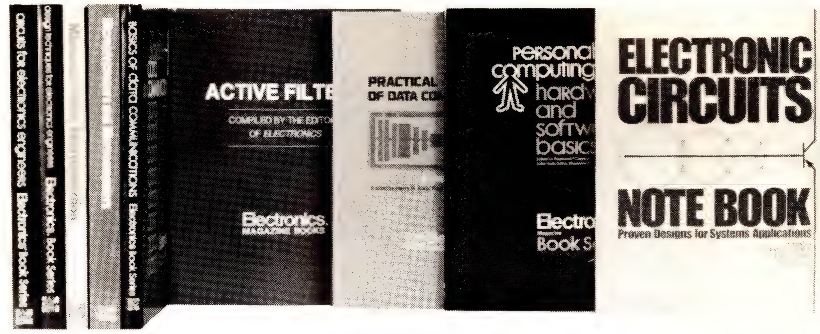
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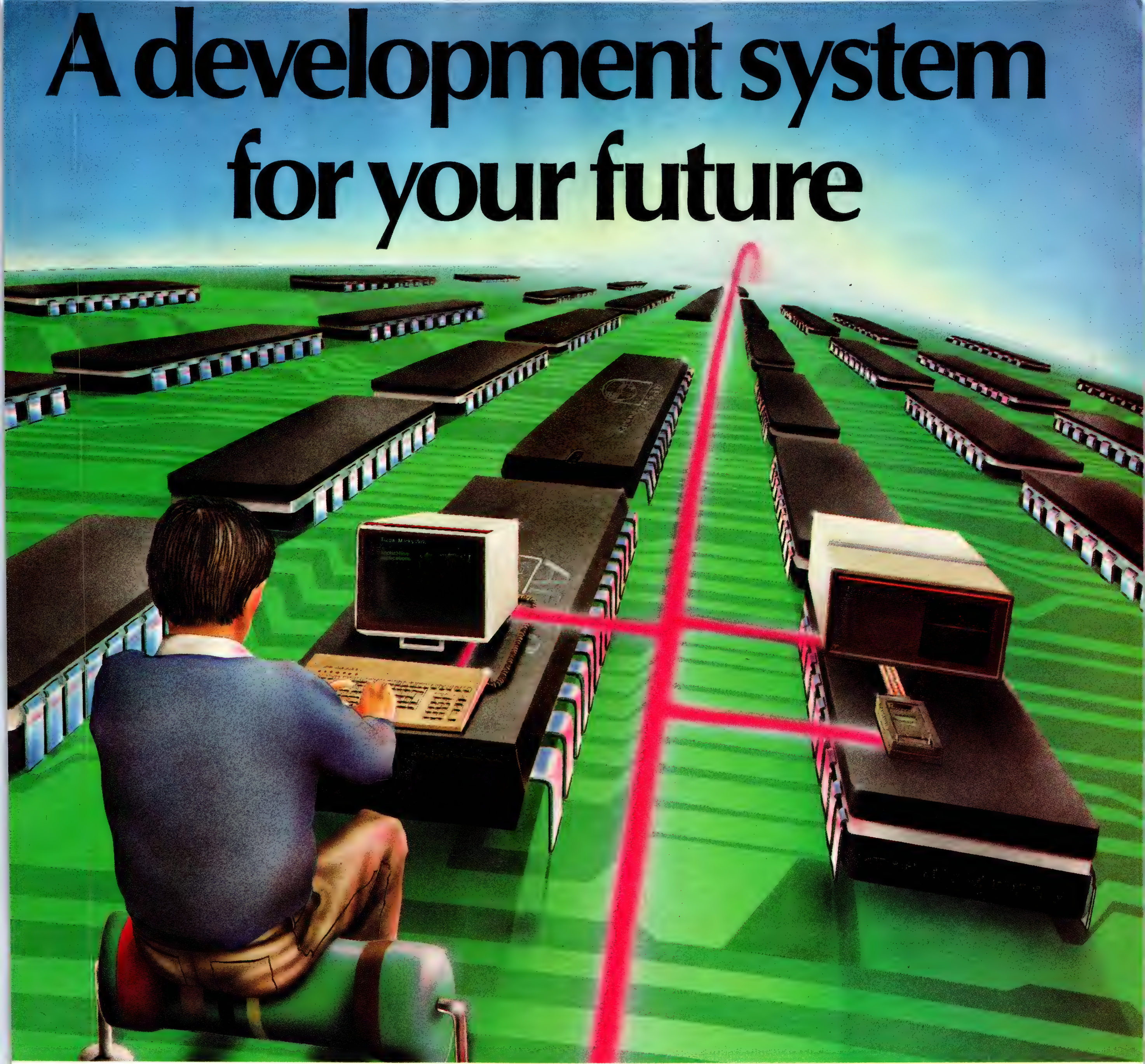
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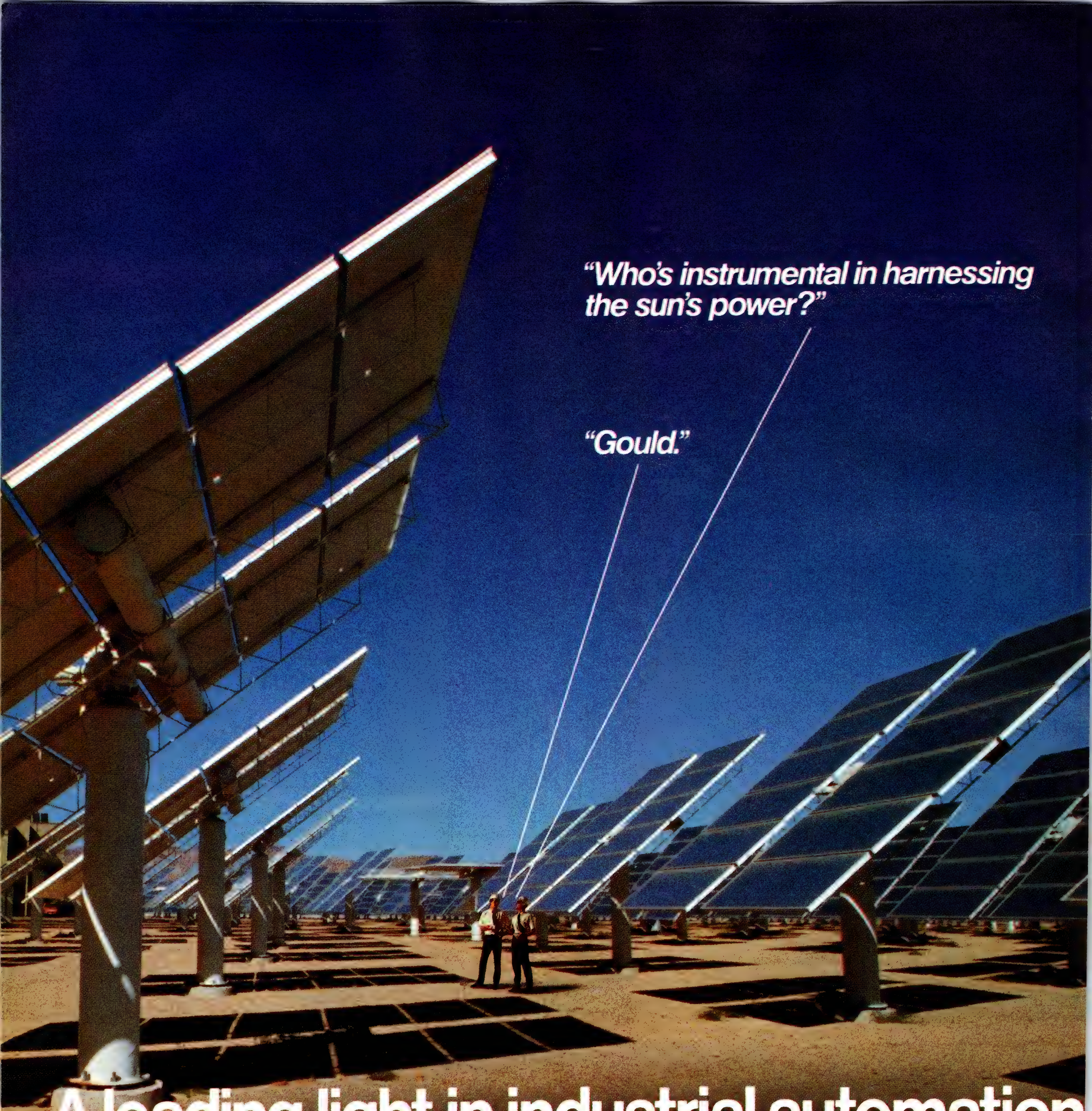

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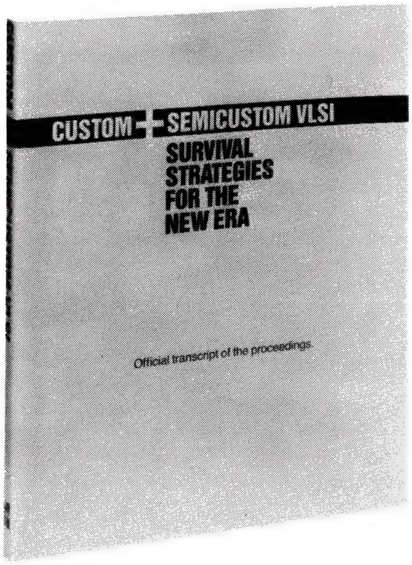
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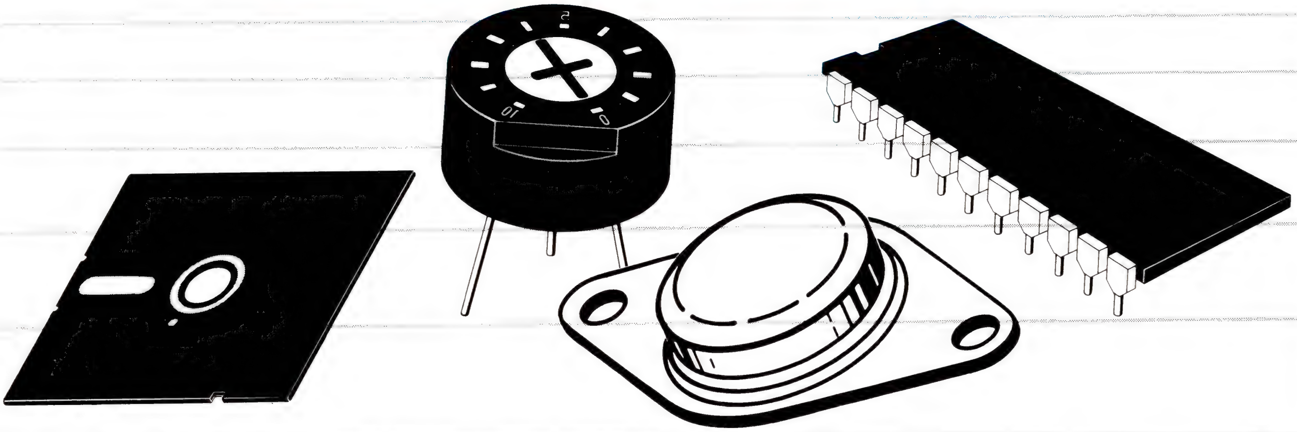

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processor, which runs at 8.0 MHz, can be switched to run at 6.0 or 7.16 MHz when the application demands.

The unit has eight add-on expansion slots, two built-in RS-232-C asynchronous communications interfaces, a printer interface, and a user memory of 1 megabyte, which is expandable to 5 megabytes. Also included is version 3.1 of the MS-DOS operating system, the GW-Basic language interpreter, and diagnostic software. Offered as options are a 60-megabyte cartridge-tape backup and a color monitor.

A basic system sells for $4,340. Units are available now.

Sperry Corp., Information Systems Group, P. O. Box 500, Blue Bell, Pa. 19424.
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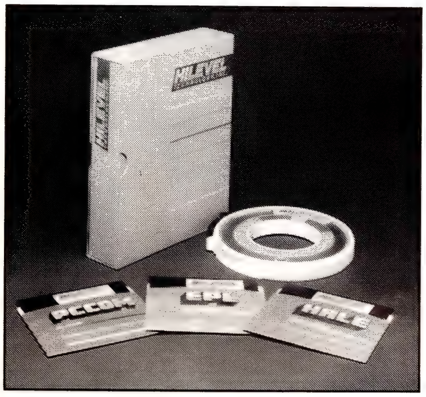

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REAL-TIME C EXECUTIVE RUNS ON AT&T SYSTEMS

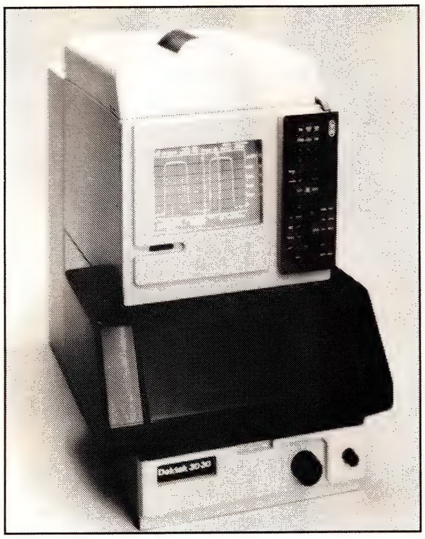
C Executive, a real-time operating system that can be contained in a ROM chip, is available for AT&T's Unix Microsystem family of products built around the 32-bit WE32100 CPU. A fully preemptive task scheduler, C Executive supports multiple-user terminals and requires only main memory to run multiple C programs.

C Executive works well as a design tool for using the Unix operating system just as a development environment or as the operating system for application software. Applications can be tested under Unix before execution under C Executive. The company recommends C Executive for applications ranging from data acquisition to PBX systems, robotics, and cardiac monitors. The single-unit binary price for C Executive is $500. A real-time file system that supports both contiguous and noncontiguous files is $750 more. A complete run-time portable C library is also included.

JMI Software Consultants Inc., 904 Sheble La., P. O. Box 481, Spring House, Pa. 19477. Phone (215) 628-0846 [Circle 361]

SYSTEM DETERMINES HYBRID'S PROFILE

The Dektak 3030 surface-profile and step-height measuring system makes profiles up to 131 μm high for thick-film hybrids and optical applications. For ultra- and very large-scale integration production, it can measure steps of less than 100 Å. Standard features include stylus pressure that is programmable from the keyboard, down to 1 mg for measuring soft materials; a sample stage that will take wafers up to 6 in. in diameter; and solid-state zoom optics of 35× to 200× magnification. Standard analytical software includes programs for calculating average roughness, average and maximum height, and area and circumference. Pricing depends on the customer's requirements; the profiler will be available in December.



Sloan Technology Corp., 602 E. Montecito St., Santa Barbara, Calif. 93103.
Phone (805) 963-4431 [Circle 367]

DEDICATED MACHINE INSPECTS ARTWORK

The circuit-board inspection machine (CBIM) for examining phototools contains a patented optical imaging system that is dedicated to the inspection of silver halide and diazo artwork. The CBIM's resolution is accurate to 0.0003 in. It identifies over 30 types of defects, including broken conductors, "mouse-bites," shorts, voids, and pad and land defects. It can be interfaced to existing systems for computer-aided design and manufacturing as well as for computer-integrated manufacturing. Size and location of defects are printed out, and process-control feedback of circuitry line widths is performed automatically. Pricing for a CBIM starts at $200,000, with delivery requiring four to six months.

Automation Engineering Inc., 11689 Sorrento Valley Rd., San Diego, Calif. 92121. Phone (619) 481-1295 [Circle 368]

DC SOURCE-MONITOR FINDS CURRENT LEAKS

The HP 4141B dc source-monitor measures semiconductor parameters at a sweep speed of 51 points in 490 ms. Its high accuracy and resolution—current monitor resolution is 50 fA and voltage resolution is 100 μV—enable such measurements as the leakage current of a MOS gate or the resistivity and sheet resistance of a wafer. There are four stimulus-measurement units within the HP 4141B, and each unit is the equivalent of four instruments. A unit can source and measure up to 100 mA and 100 V. By using the units and the two additional built-in voltage sources and monitors, the user can make a complete set of dc semiconductor wafer measurements with one probing.

The instrument is designed to be used with a computer over the IEEE-488 bus. The price of the HP 4141B is $15,300, and delivery takes about seven weeks.

Hewlett-Packard Co., Inquiries Manager, 1820 Embarcadero Rd., Palo Alto, Calif. 94303 [Circle 370]

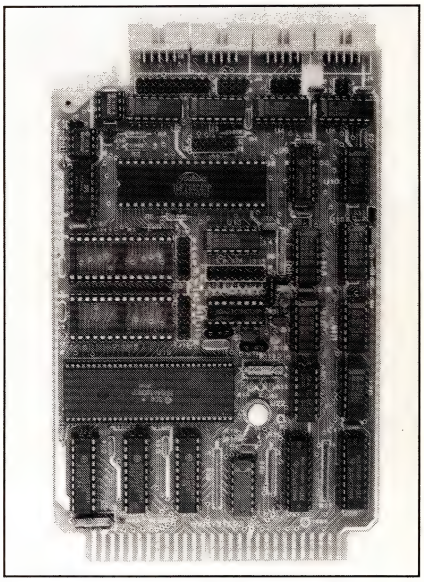
8-BIT COMPUTER USES THE HD64180

A single-board computer offers 8-bit systems integrators many of the advantages of 16-bit microprocessors, but remains fully compatible with software developed for Z80-based systems. The combination of more processing power and software compatibility is made possible by the use of Hitachi's 8-bit HD64180, an enhanced version of the widely used Zilog Z80 microprocessor.

The Hitachi 8-bit microprocessor expands normal Z80 direct memory addressing to 512-K bytes. The CPU has two direct-memory-access channels, two serial channels, automatic dynamic refresh generation, a wait-state generator, a watchdog timer, three sleep modes, two 16-bit timers, four RS-232-C/422 serial channels, and hardware multiply.

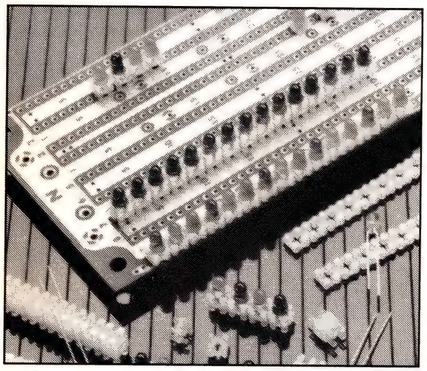
The SBC5 computer board is available in two versions: an all-CMOS system and a configuration for n-MOS/TTL buses. The CMOS board, designated LPM-SBC5, costs $450 for a 4-MHz model, while the n-MOS/TTL version is priced at $395. Both are now available.

WinSystems Inc., Box 121361, Arlington, Texas 76012.
Phone (817) 247-7553 [Circle 379]



MATERIALS

LED MOUNTS. These T-1 LED mounts fit tubular and other standard LEDs and also allow for variation among different manufacturers' products. Molded in one-piece strips of 15 stations, T-1 strip-mounts can be used for entire arrays. Otherwise, couplings between segments can be cut. A total of 60 different elevations and spacing sizes are available. Recommended applications include fault and activity indicators for pc-board-edge mounting or flush panel displays. Standard spacing is 0.200 in., and elevations range from 0.60 to 0.350 in. to accommodate a variety of lead configurations and lead spacings. A polarity indicator is incorporated for uniform lead orientation, and standoffs allow for board washing and removal of solder residue. T-1 strip-mounts sell for $91.50 per 1,000 units in quantities of 10,000. Individual T-1 LED mounts sell for $31.25 in the same quantities. Both are available from stock.



Bivar Inc., 4 Thomas St., Irvine, Calif. 92718. Phone (714) 951-8808 [Circle reader service number 421]

CONFORMAL COATING. Uralane 5750-A/B(LV) urethane conformal coating meets MIL-I-46058C and weapons specifications 12956 and 18941. It demonstrates excellent flexibility from –80°C to +125°C as well as extremely low outgassing properties in outer-space and high-vacuum environments, the manufacturer says. Coatings created with this material can be repaired by mechanical and hot-knife methods. Uralane 5750-A/B(LV) is available in pail kits for metered mixing and dispensing, and case lots of quarts and gallons.

Furane Products Co., 5121 San Fernando Rd. W., Los Angeles, Calif. 90039.
Phone (818) 247-6210 [Circle 422]

DELIVERY SYSTEM. The JS100 series of modular component-selection systems comprises several manual or powered turntables, self-stacking carousel trays, and various accessories. LEDs are set into the system's height-identification tower at four different levels, showing the operator the correct carousel tray

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Signamatic Corp., 2007 Bridgeport Ave., Milford, Conn. 06460.
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Preci-Coat SA, Bliss, Barefoot & Associates Inc., U. S. Representatives, 500 Fifth Ave., New York, N. Y. 10110.
Phone (212) 840-1661 [Circle 424]

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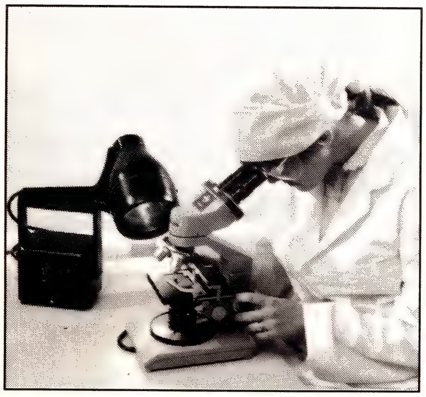
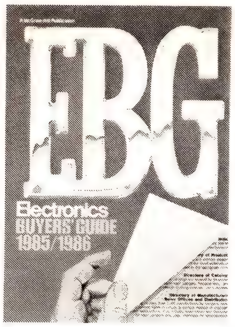
Fiberguide Industries, 33 Poplar Dr., Stirling, N. J. 07980.
Phone (201) 647-6601 [Circle 425]

INSPECTION LAMP. The Blak-Ray model B-100Y 100-W inspection lamp features a yellow filter for high-contrast illumination for surface inspection of semiconductor wafers. The yellow filter blocks wavelengths shorter than 500 nm, transmitting only wavelengths beyond photoresist-exposure levels. Optimum intensity at the center of the spot covers a





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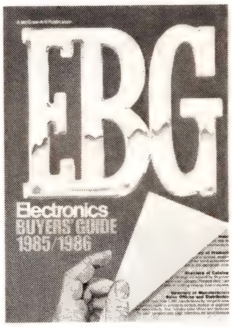

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MATERIALS

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GTE Precision Materials, Special Products Division, Portsmouth Ave., Exeter, N. H. 03833. Phone (603) 772-4331 [Circle 427]

CABLE. Flexbond cable was developed to replace rigid-flex pc-board connections in such applications as connections between mounted cards on different planes. When the company's Nanowire is used in Flexbond cable assemblies, it creates connections between boards using surface-mounted devices. The motherboard connectors can be removed if damaged without the need for modifying the flex-cable board assembly. The customer can specify the space between wires.

Advanced Performance Technology, 13207 Wentworth St., Arleta, Calif. 91331.
Phone (818) 768-1832 [Circle 428]

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Celanese Engineering Resins, Information Services Center, 114 Mayfield Ave., Edison, N. J. 08818.
Phone (201) 635-4339 [Circle 429]

CASTING MATERIAL. Tra-Cast 3010 epoxy resin features a low exothermic heat rise, recommending it for casting, potting, and impregnating heat-sensitive components. It offers near-zero shrinkage in large mass castings. Tra-Cast 3010 cures at room temperature to a flexible, clear solid that offers good electrical insulation and weatherability. When used to coat printed circuits or to embed components, it permits easy repair or replacement. Tra-Cast 3010 is available from stock in premeasured Bipax packages.

Tra-Con Inc., Resin Systems Division, 55 North St., Medford, Mass. 02155.
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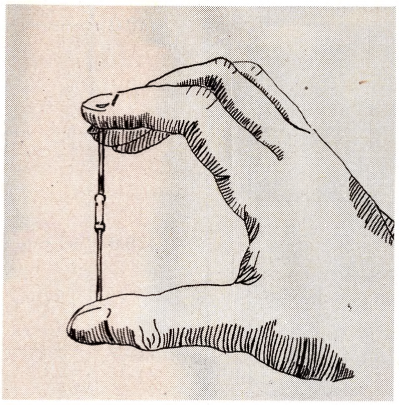

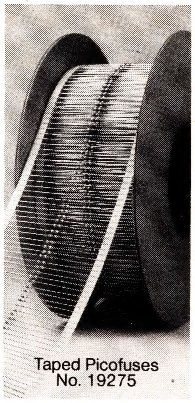

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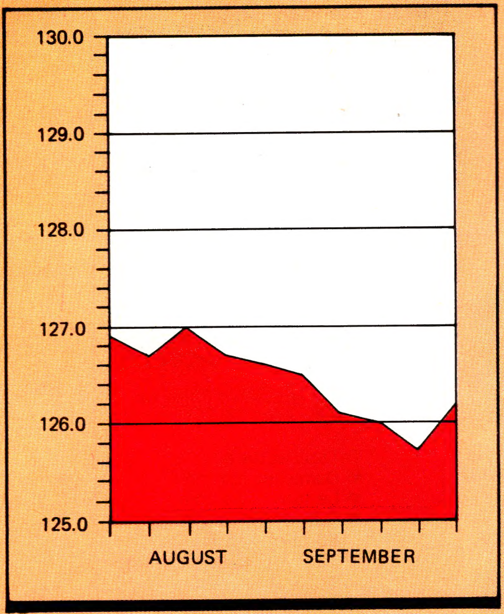

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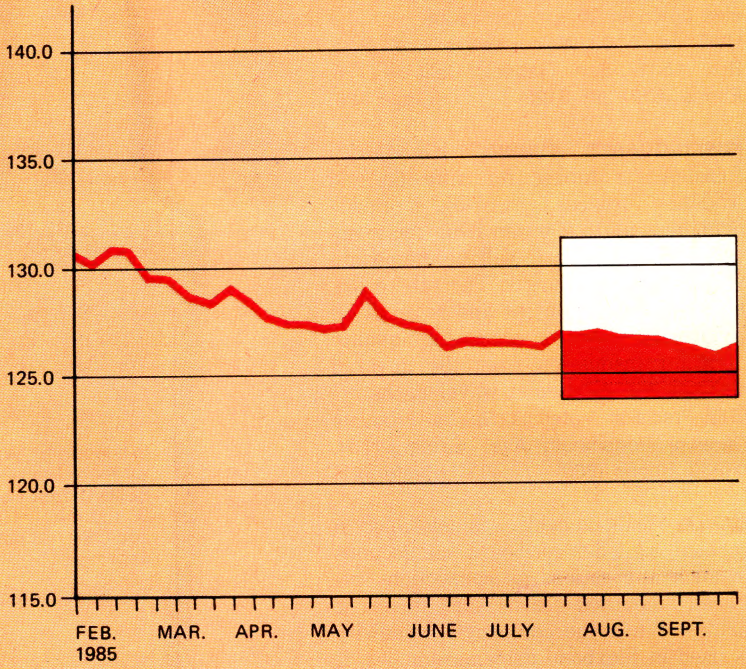

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U. S. GENERAL ECONOMIC INDICATORS

	August 1985	July 1985	August 1984
Index of leading economic indicators	170.1	169.0	164.4
Budgeted outlays of the federal government ($ billions)	83.621	78.012	88.707
Budgeted outlays of the Department of Defense ($ billions)	23.209	22.140	20.059
Operating rate of all industries (% capacity)	78.0	77.9	80.5
Industrial-production index	124.8	124.4	123.5
Total housing starts (annual rate in thousands)	1,749	1,647	1,590

U. S. ELECTRONICS SHIPMENTS

Shipments ($ billions)	August 1985	July 1985	August 1984
Communications equipment	5.301	4.865	4.683
Radio and TV receiving equipment	0.910	0.901	0.874
Electronic and electrical instruments	4.636	4.829	4.504
Components	3.257	3.159	3.934

A 2½% surge in shipments of U. S.-made electronics equipment in August pushed the *Electronics* Index up a healthy 0.4%, its first upswing in a month. Even with the boost, though, industry performance as measured by the index remains more than 4% below levels of last August. And even the good news is not all good: shipments were just 0.8% ahead of a year ago. In addition, electronics industry's improved shipment rate in August, though a welcome relief, could not make up completely for the 4% drop in shipments in July. As a result, the month's shipments of electronics products were over $150 million below June's $14.3 billion level.

Except for a dramatic 4% decline in shipments of instruments, each segment of the electronics industry performed well. Makers of communications equipment had the single biggest gain in shipments at 9%, bringing communications-equipment sales to their highest point since last December and 13.2% above the August 1984 level. The hard-hit components industry registered a 3.1% gain in shipments in the month, which could signal a firming trend.

Sperry Technology: Preparing for tomorrow's challenges

Sperry's Space Systems Division is preparing for tomorrow's challenges. We are providing technology for the Space Station and Space Shuttle. We are developing technology for a number of other Space based projects. We need experienced engineers to join us in Phoenix, a fast growing city which offers you a year-round outdoor lifestyle. We have openings in the following areas:

Attitude Control System Engineers

ACS Design

In this position you will be responsible for the development of system requirements and specifications and for the definition of interface documents and system hardware. You will develop error budgets, flowdowns of requirements and the process for designing attitude control systems (ACS). Experience in ACS system design and trade studies is desired for this position.

Attitude Determination

This position calls for a control systems engineer with a background in attitude determination, reference and control. You will develop the algorithms for attitude reference and define ACS interfaces with the Attitude Reference System. Your experience should include analysis of Attitude Reference Systems and knowledge of inertial measurement components.

Control Systems Design

Challenging positions exist at all levels of experience in spacecraft attitude control, pointing systems, and electromechanical servomechanism design. To qualify for these assignments you will need five or more years experience in the synthesis of servomechanisms. You will participate in the development of control systems for high gain antennas, solar array drives and momentum exchange devices. Experience in the conceptual design, synthesis, analysis and simulation of control systems for orbiting applications is desirable.

Test Systems Engineers

Hardware and software positions are available for the development of test systems for spacecraft attitude control systems and components. Positions open include test system design, test hardware development, test software development and system simulation. To qualify for software and systems positions, you should be familiar with HP-1000 and HP-9800 series hardware and software or with the MC6800 microprocessor, Unix operating system, "C", and ATLAS languages. Test hardware development will require a background in analog or digital circuit design.

Integration/Test Engineers

In this assignment you will prepare for and execute the integration and test of spacecraft attitude control components and spacecraft mechanisms. Activities will include test planning and procedure generation, test fixture specification, test monitoring, failure investigation and orbital anomaly analysis. You should have experience in integration and testing of complex electromechanical systems and be familiar with spacecraft attitude control components and automated test systems.

Electronic Engineers

Assignments at all levels involving synthesis, analysis and development of high-reliability aerospace hardware. You will be involved with the application of analog and digital electronics in both signal and power handling circuits. Hands-on hardware experience is desired.

Electro Optics

Lead the development of new space systems products, including optical data communications interface. You should have three or more years design experience in electro-optics systems and have a fundamental knowledge of optics, sensors and detectors. System analysis capability is desirable.

All positions require U.S. citizenship and a BS degree in Engineering, Physics, Mathematics or Computer Science.

Take the challenge. Send your resume and salary history, in confidence, to Clarence Williams, Sperry, E-E630, P.O. Box 21111, DV5C, Phoenix, AZ 85036.

SPERRY

Equal Employment Opportunity/Affirmative Action Employer

2,000 sharper-than-ever characters all on a portable LCD display.

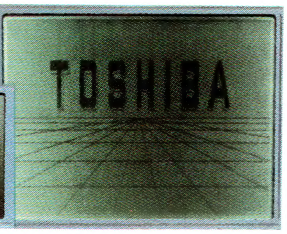
Toshiba's newest LCD modules give you 640 × 200 dot displays in a choice of two viewing sizes. One is approximately the size of a magazine, and the other about half that size.

Both sizes put an enormous amount of information on view . . . an array of 80 characters × 25 lines. But still bulk and power consumption are at a minimum. Battery powered, these slim modules interface with various systems through LCD controller without renewing software.

Toshiba's advanced technology has also eliminated surface reflection and developed a sharper contrast which gives a brighter and easier to read viewing screen. And for low light or dark viewing an optional backlightable LCD is available.

These versatile LCDs are ideally suited for applications as displays for personal computers, POS terminals, portable word processors and other display terminals. You can also look to Toshiba with confidence for a wide range of sizes and display capacity to suit your LCD requirements.

TLC-363



TLC-402

Specifications

		TLC-402	TLC-363B
Display			
Number of Characters		80×25 (2,000 characters)	80×25 (2,000 characters)
Dot Format		8×8, alpha-numeric	8×8, alpha-numeric
Overall Dimensions (W × H × D)		274.8×240.6×17.0 mm	275.0×126.0×15.0 mm
Maximum Ratings			
Storage Temperature		−20° – 70° C	−20° – 70° C
Operating Temperature		0° – 50° C	0° – 50° C
Supply Voltage	V_{DD}	7 V	7 V
	$V_{DD} - V_{EE}$	20 V	20 V
Input Voltage		$0 \leq V_{IN} \leq V_{DD}$	$V_{SS} \leq V_{IN} \leq V_{DD}$
Recommended Operating Conditions			
Supply Voltage	V_{DD}	5±0.25V	5±0.25V
	V_{EE}	−11±3V Var.	−11±3V Var.
Input Voltage	High	V_{DD} − 0.5V min.	V_{DD} − 0.5V min.
	Low	0.5V max.	0.5V max.
Typical Characteristics (25°C)			
Response Time	Turn ON	300 ms	300 ms
	Turn OFF	300 ms	300 ms
Contrast Ratio		3	3
Viewing Angle		15 – 35 degrees	15 – 35 degrees

Design and specifications are subject to change without notice.

TOSHIBA

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